

Compal Confidential

Broadwell M/B Schematics Document

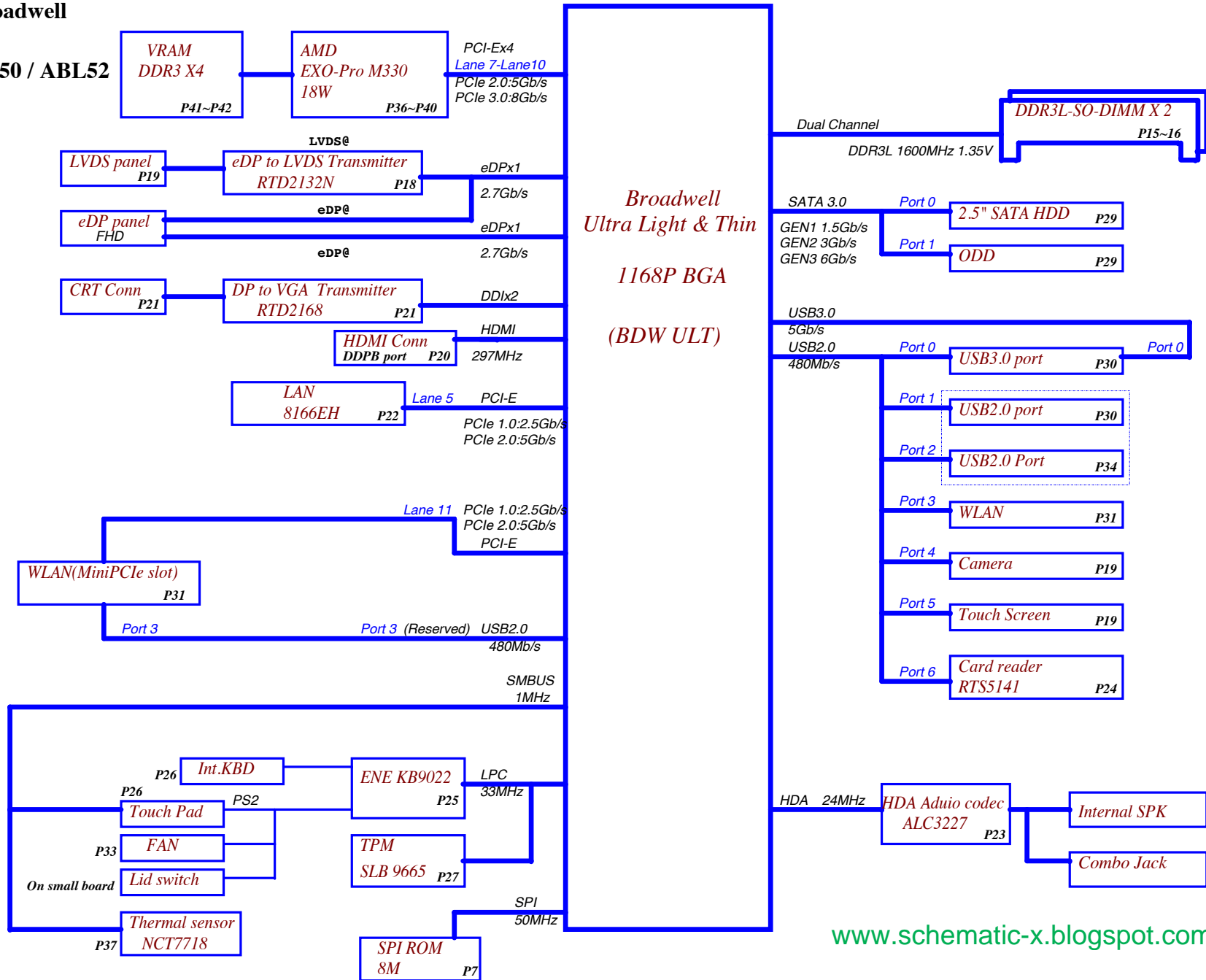
Intel ULV Processor with DDRIII

Date : 2015/01/31

Version 0.3

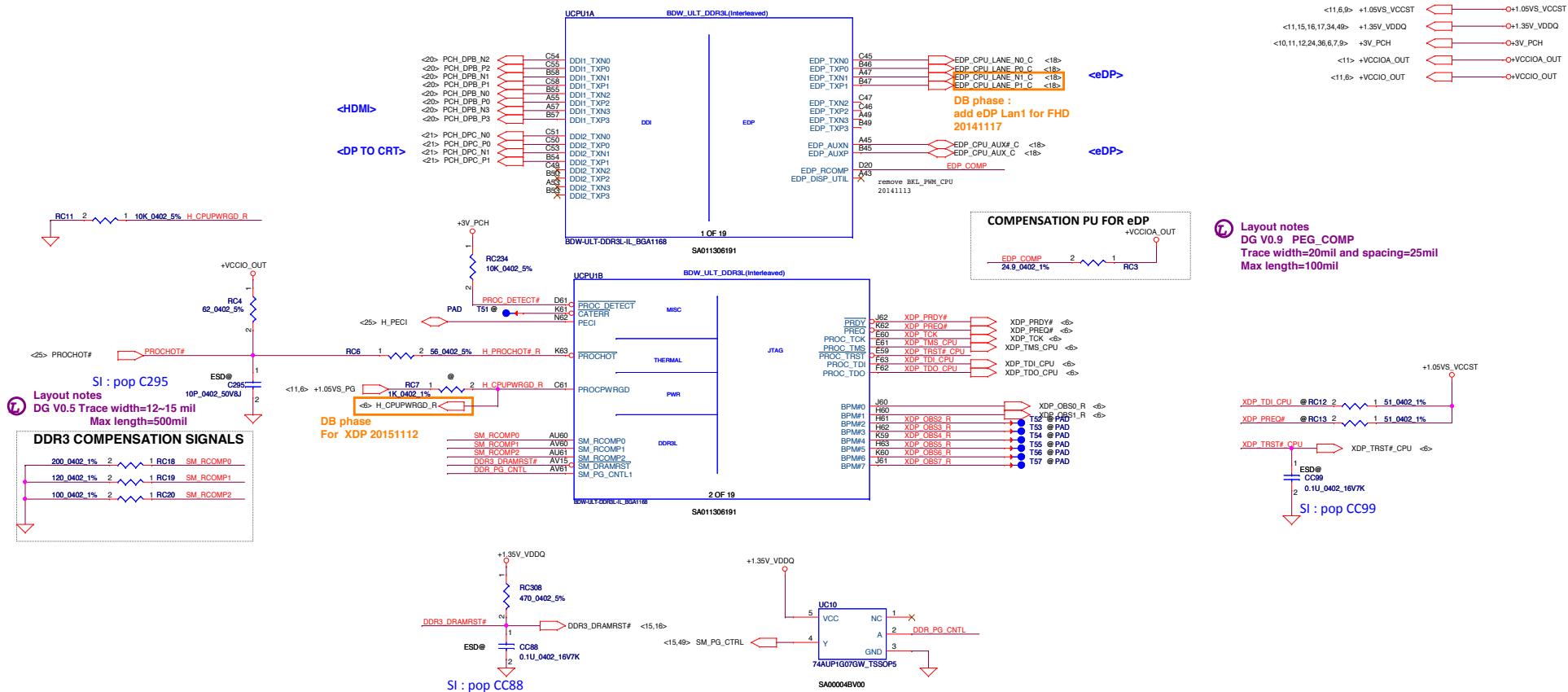
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	
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				Size B	Rev 0.1
				Document Number	
				LA-C701P	
				Date: Saturday, January 31, 2015	Sheet 1 of 61

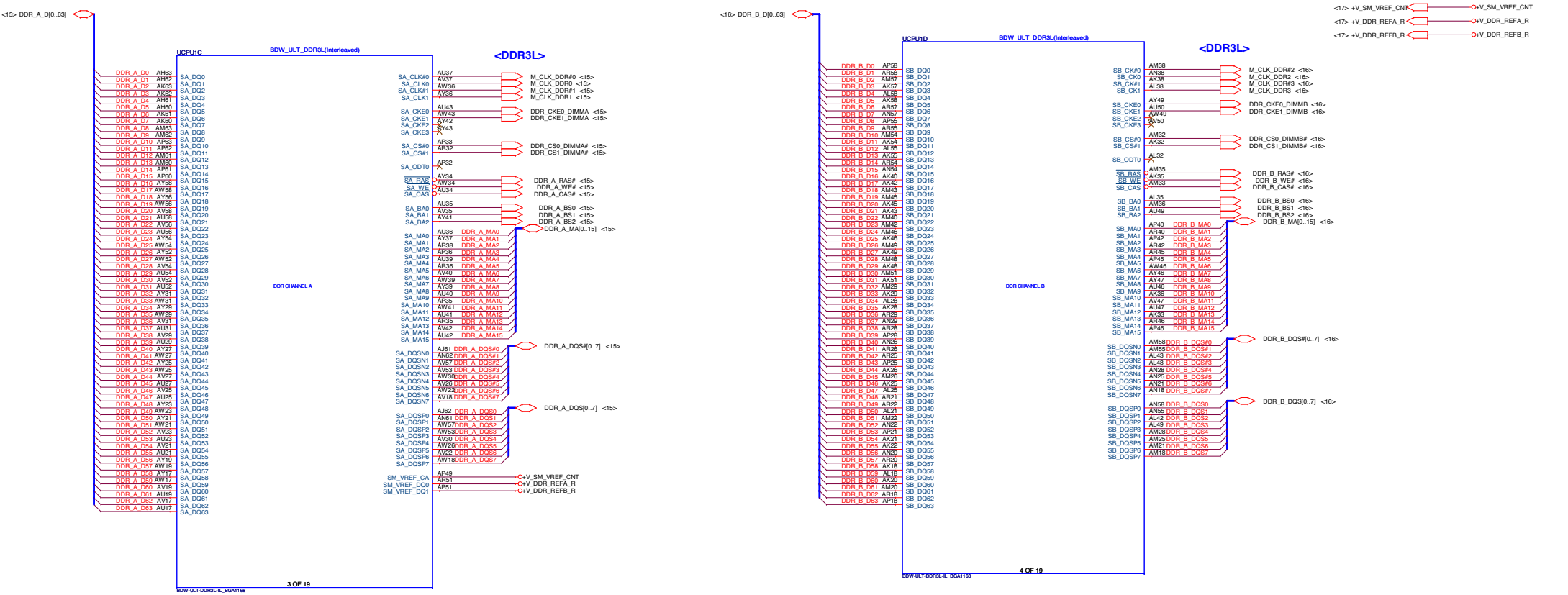
File Name : AHL50 / ABL52
LA-C701P



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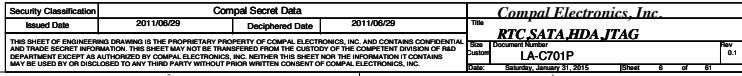
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Block Diagrams
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				Date: Saturday, January 31, 2015	Rev 0.1
				Sheet 2 of 61	

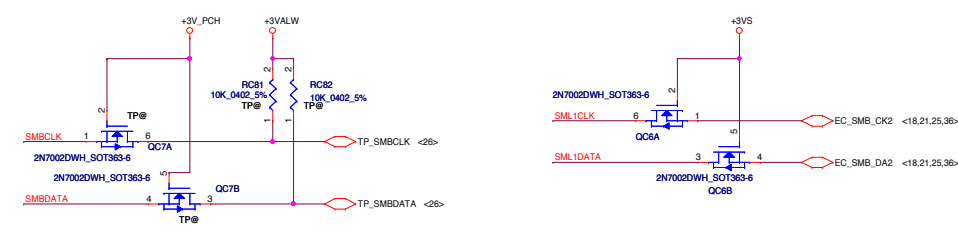
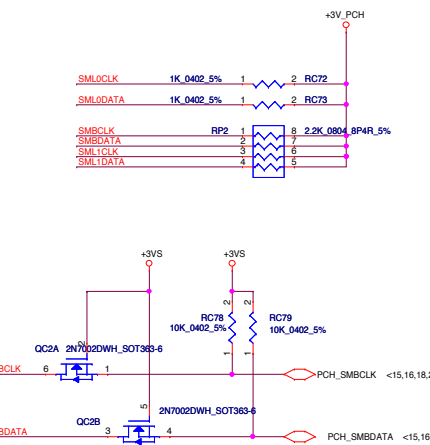
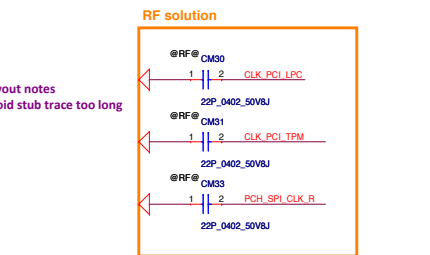
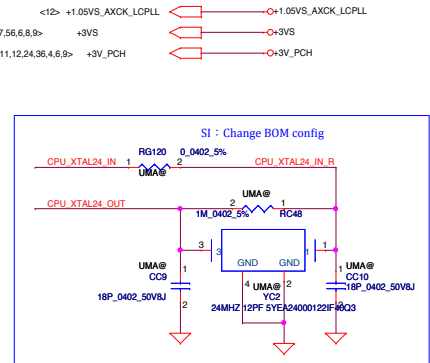




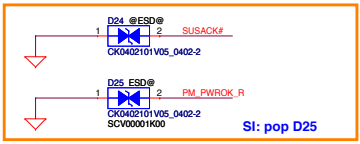
Interleaved Memory

Security Classification				Compal Secret Data		Title	
Issued Date		2011/06/29		Deciphered Date		2011/06/29	
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Date:		Saturday, January 31, 2015		Sheet		5 of 61	



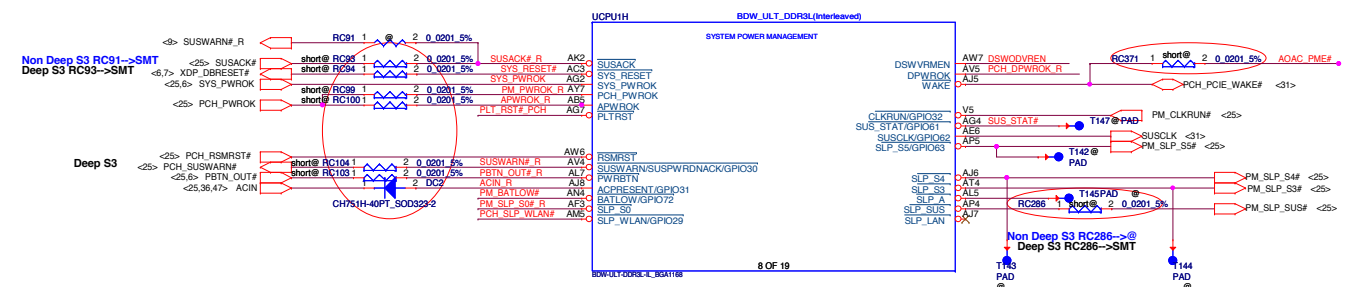


Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	CLK, SPI, SMB, LPC
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				LA-C701P	
				Date	Saturday, January 31, 2015

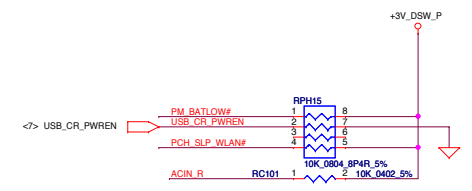
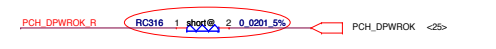
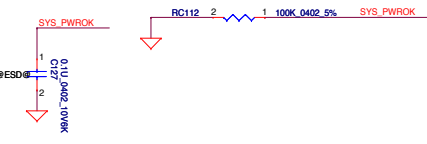
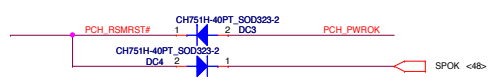
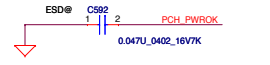
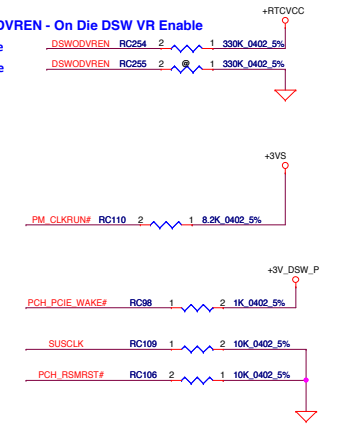


DB phase :
For ESD request
20141117

<12,28,6> +RTCVCC
<10,11,12,24,36,4,6,7,9> +3V_PCH
<12,15,16,18,19,20,21,22,23,24,25,27,31,32,33,34,35,36,37,56,6,7,8> +3VS
<12,9> +3V_DSW_P

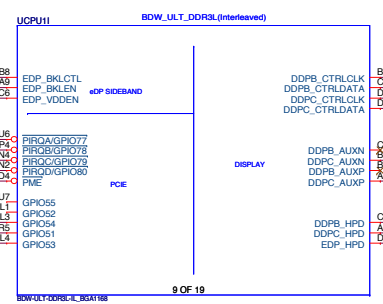
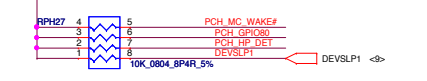
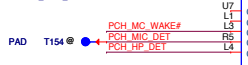


DSWODVREN - On Die DSW VR Enable
* H:Enable
L:Disable



PV:RC114,RC115,RC116,RC118,RC121,RC122
change to 0-ohm shortpad

<18,19> BKL_PWM_CPU
<25> ENBKL
<19> ENVDD_CPU
<36,9> DGPU_PWROK
<25,37,54,9> DGPU_PWR_EN
<35,9> DGPU_HOLD_RST#
<25> AOAC_PME#



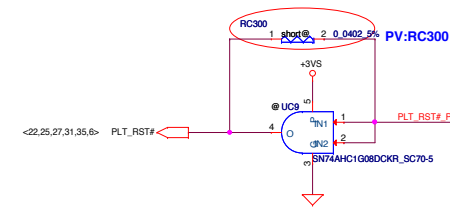
Displayport Port C Enable pin RC102 pull high +3VS

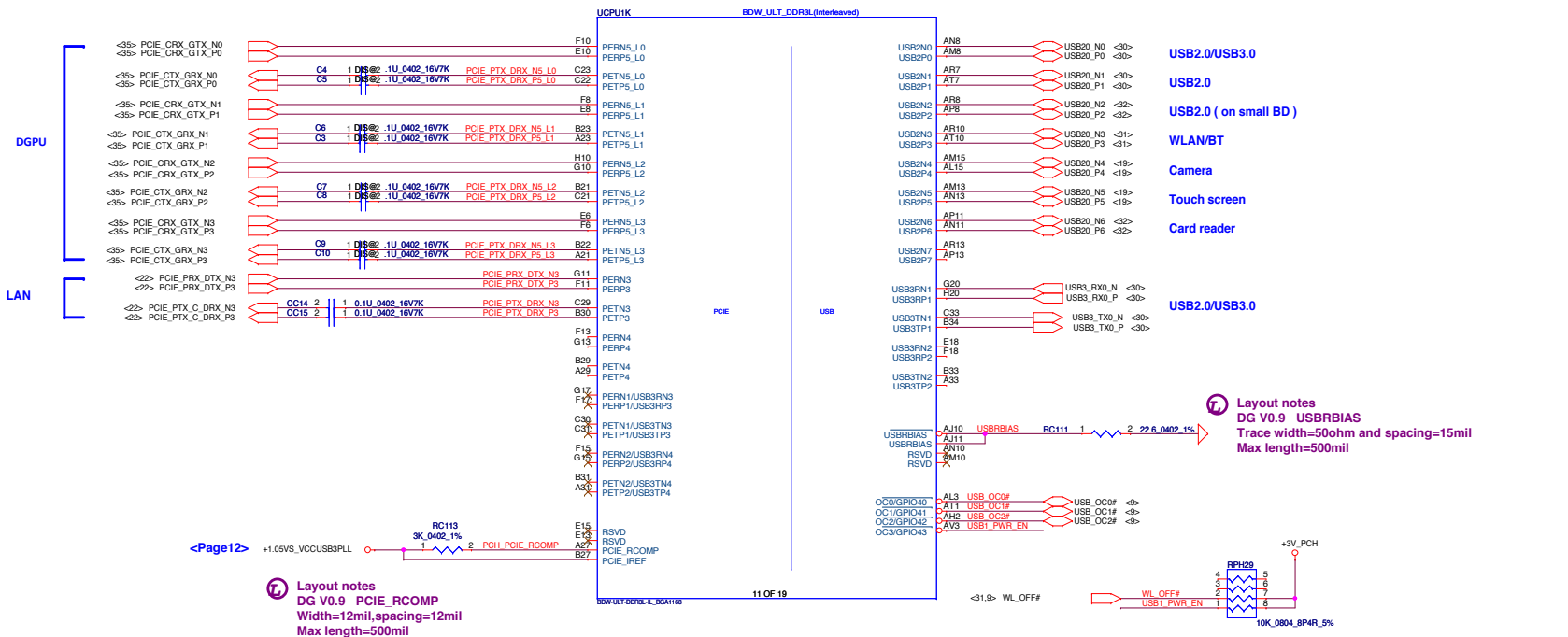
DP TO CRT (RTD2168)

DP TO CRT HPD (RTD2168)

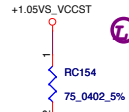
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PV:RC300 change to 0-ohm shortpad



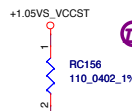


SVID ALERT



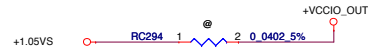
Layout notes
DG V0.5 H_CPU_SVIDALRT#
RC154 close to CPU<300mil
Max length=1000~2000mil

SVID DATA



Layout notes
DG V0.5 VIDSOUT
RC156 close to CPU<500mil
Max length=1000~2000mil

<CPU>



VCC_SENSE

<PWR VR12.6>

<VR IV and CPU>
<EDP_COMP power rail>

<51> VCCSENSE

<4,6> +1.05VS_PG

<51> VR_ON

H_CPU_SVIDALRT#

VR_SVID_CLK

VR_SVID_DAT

VR12.6PG_MCP

CPU_PWR_DEBUG

+VCCIO_OUT

+VCCIO_OUT

+VCCIO_OUT

+VCCIO_OUT

+VCCIO_OUT

+VCCIO_OUT

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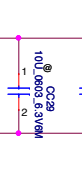
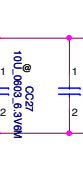
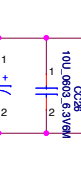
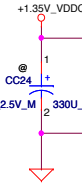
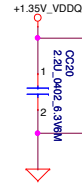
+VCC_CORE@10000mA

<34,51,52> +VCC_CORE
<15,16,17,34,4,49> +1.35V_VDDQ
<4,6,9> +1.05VS_VCCST
<4,6> +VCCIO_OUT
<4> +VCCIOA_OUT
<12,24,25,28,34,37,50,51> +1.05VS

HSW ULT POWER

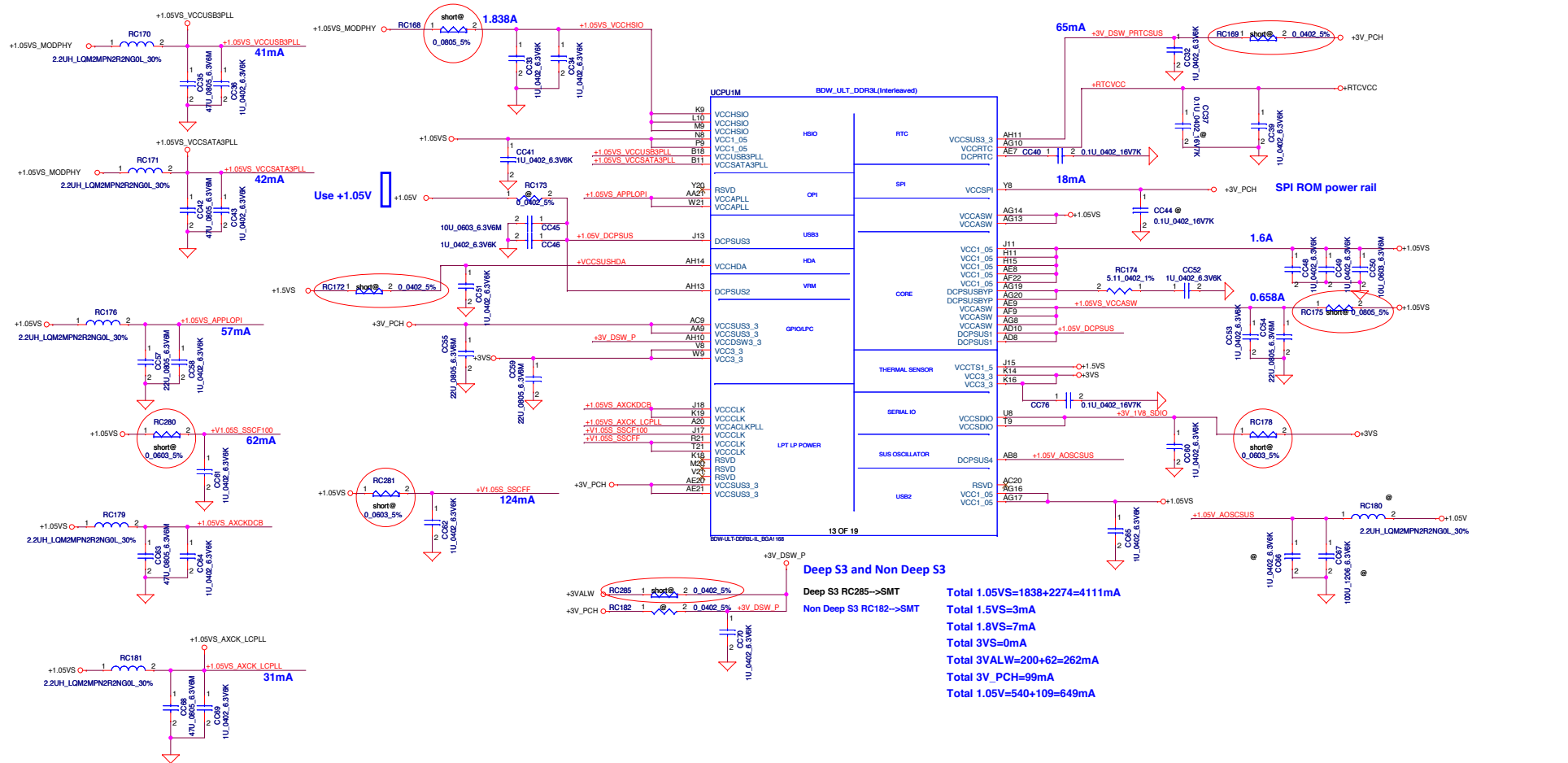
12 OF 19

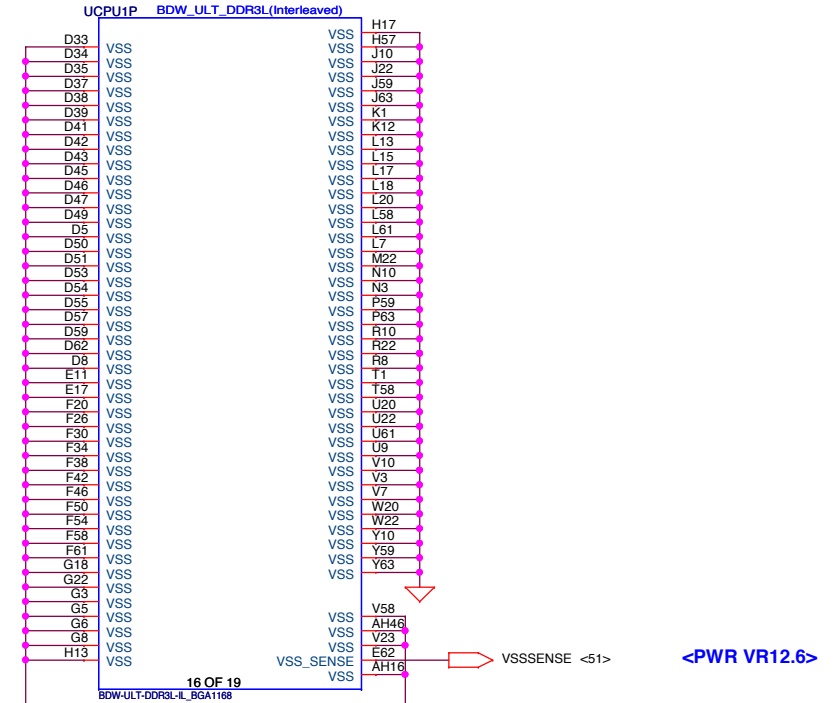
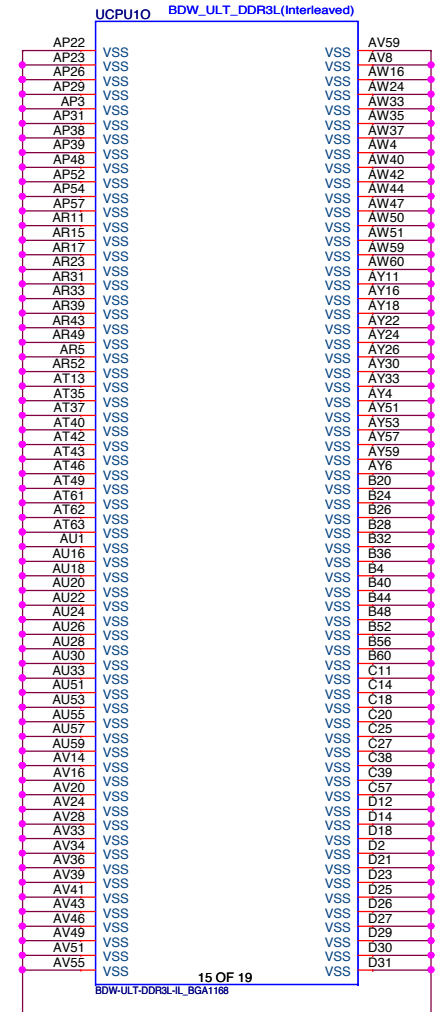
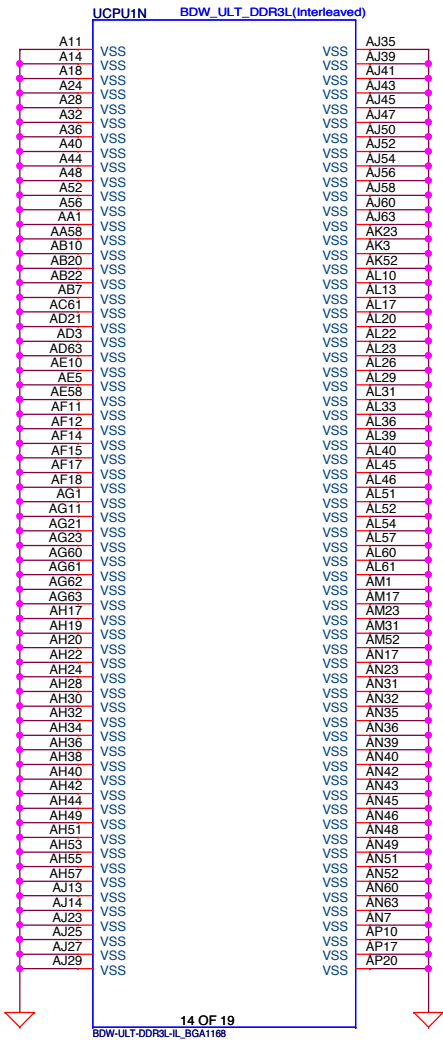
PV:RC223,RG124 change to 0-ohm shortpad



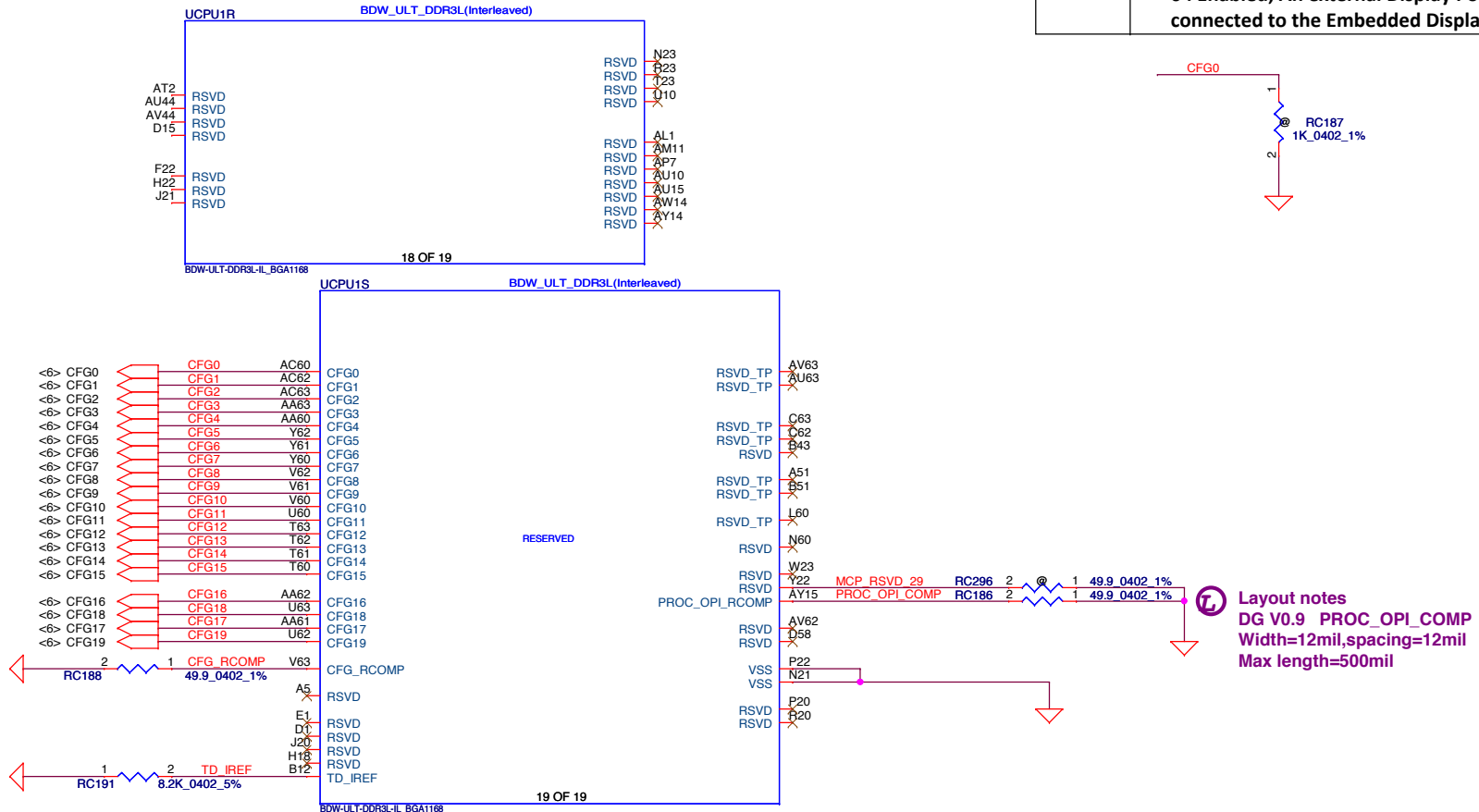
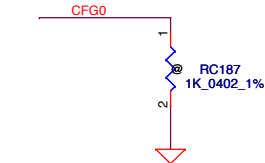
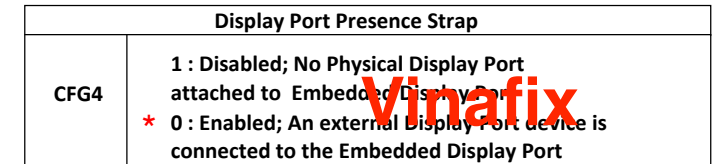
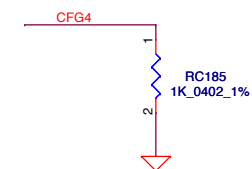
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Issued Date				2011/06/29				Title			
Deciphered Date				2011/06/29				Power			
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PV:RC168,RC172,RC280,RC281,RC285,RC196,RC175,RC178 change to 0-ohm shortpad

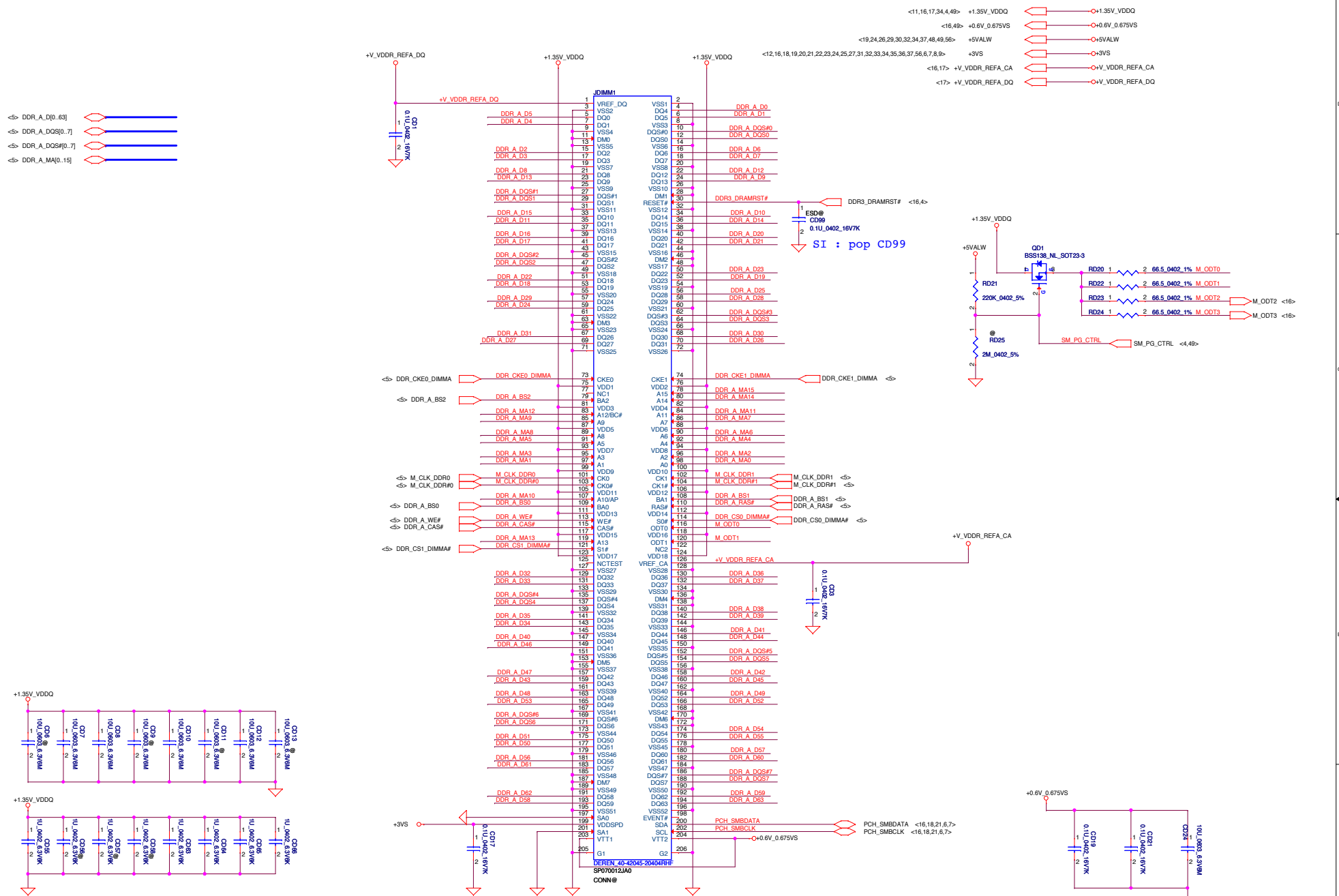


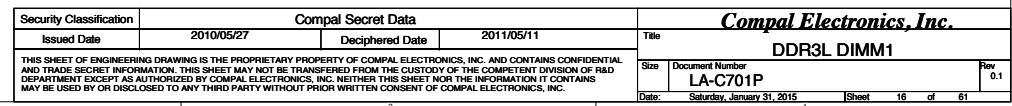


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				Document Number	0.1
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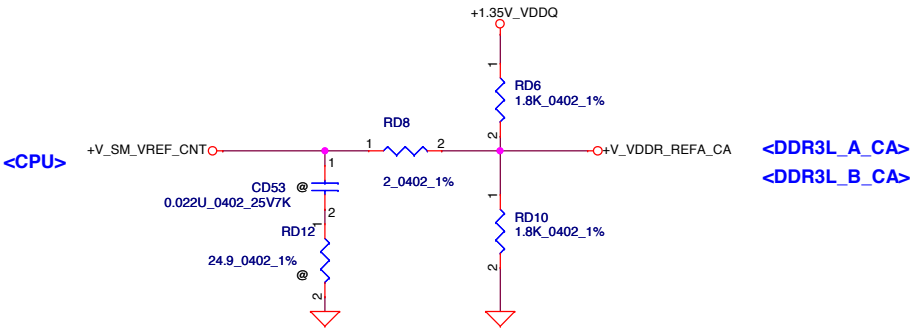
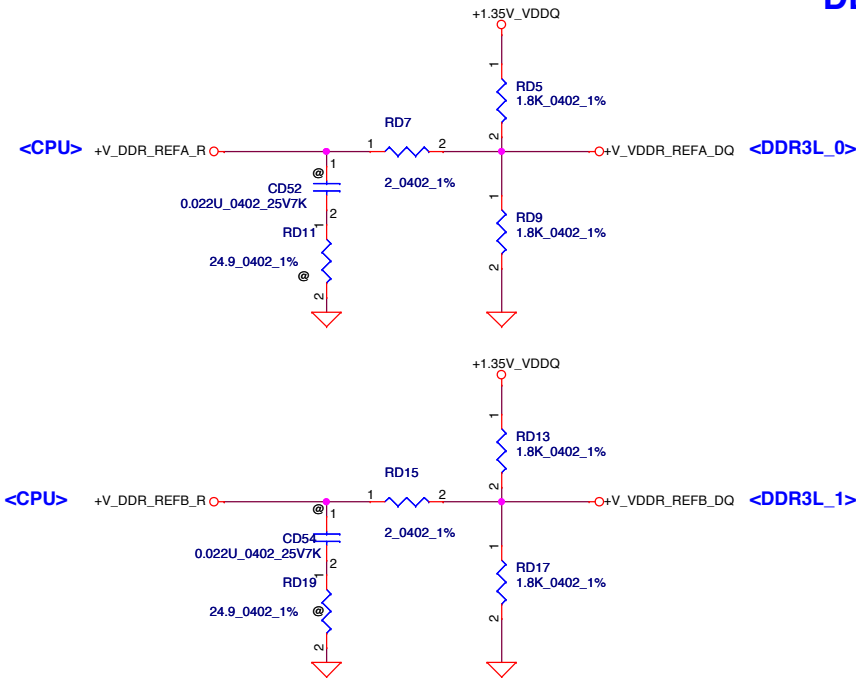


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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	RSVD/CFG	
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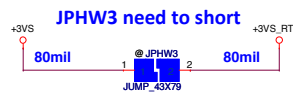


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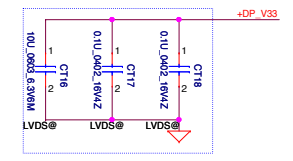


- <11,15,16,34,4,49> +1.35V_VDDQ
- <15,16> +V_VDDR_REFA_CA
- <5> +V_SM_VREF_CNT
- <5> +V_VDDR_REFA_R
- <15> +V_VDDR_REFA_DQ
- <16> +V_VDDR_REFB_DQ

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Layout notes
CT16-CT18 Close to Pin3



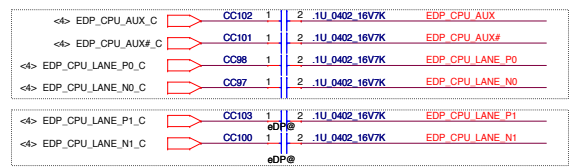
SWR / LDO Mode select		
	LDO	SWR
2132S	Do not support	mount LT7
2132N	Use 0 ohm	mount LT7

※ If use 2132N, please select LDO mode as default.

RTD2132 SMBus revrse to PCH

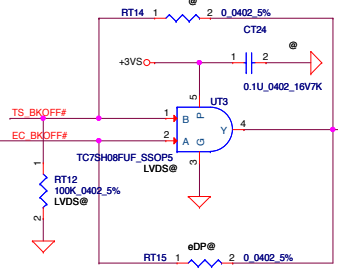


Layout notes
CC97~CC102 must closed to connector



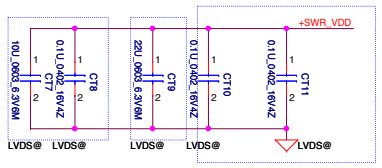
<CPU>

DB phase :
add eDP Lan1 for FHD
20141117

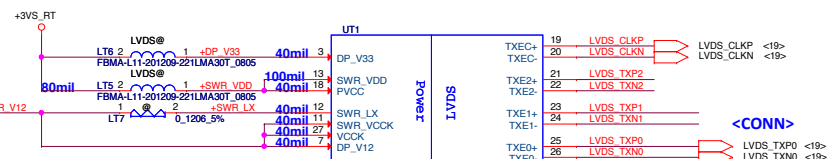
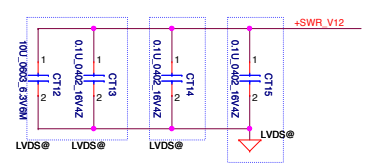


<RTS2132>
<EC CTRL>

Layout notes
Close to LT5 Pin18 Pin13



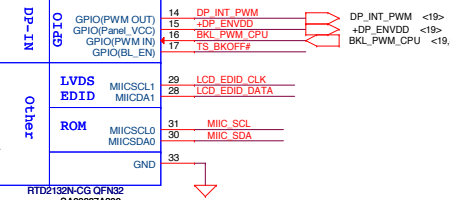
Layout notes
Close to Pin11 Pin27 Pin7



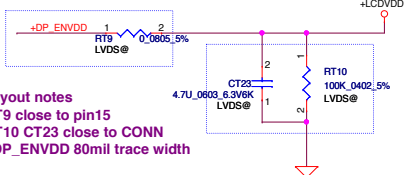
<SI> LT7 change to 0 ohm short pad
use LDO mode translator only

<CPU CTRL>

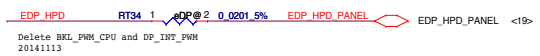
RTD2132S



Layout notes
RT8 close to pin8



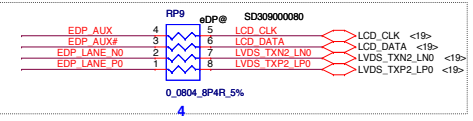
Layout notes
RT9 close to pin15
RT10 CT23 close to CONN
+DP_ENVDD 80mil trace width



<CPU by PASS eDP>



<eDP to connector>

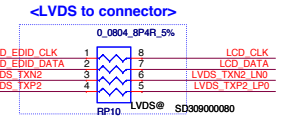


Layout notes
RP6 RP9 RP10 must closed to connector



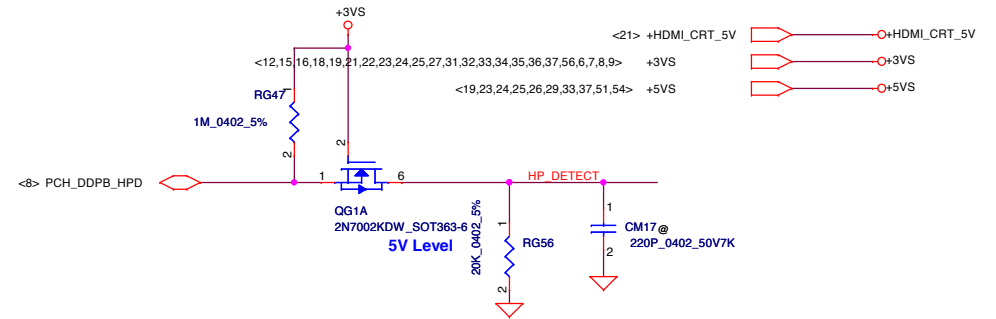
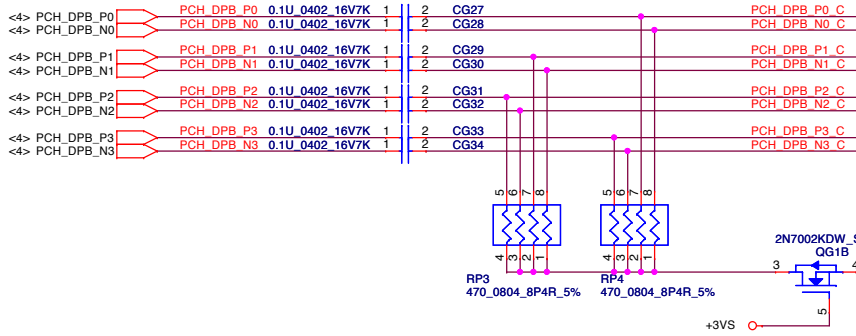
DB phase :
add eDP Lan1 for FHD
20141117

Layout notes
RT16~RT19 must closed to connector

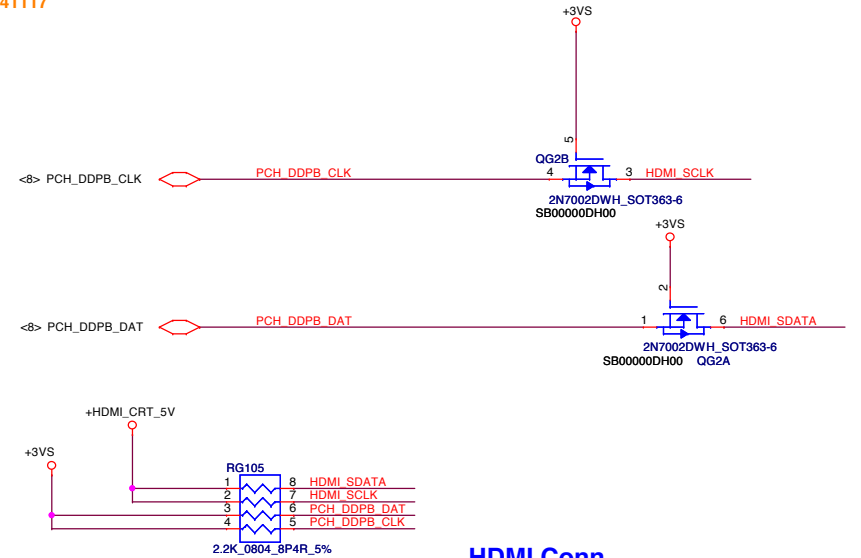
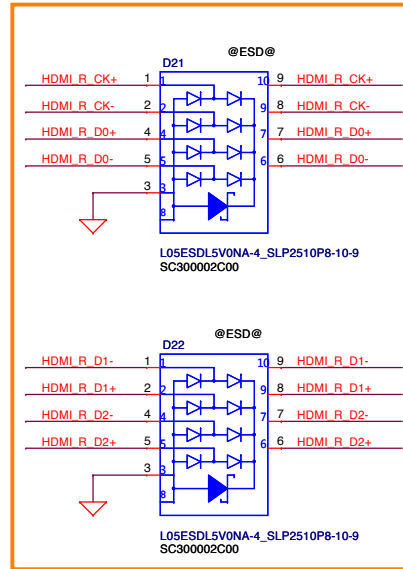


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/3/1	Deciphered Date	2015/3/1	Title	LVDS Translator-RTD2132N
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				Rev	D.1
				Date	Saturday, January 31, 2015
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<CPU>



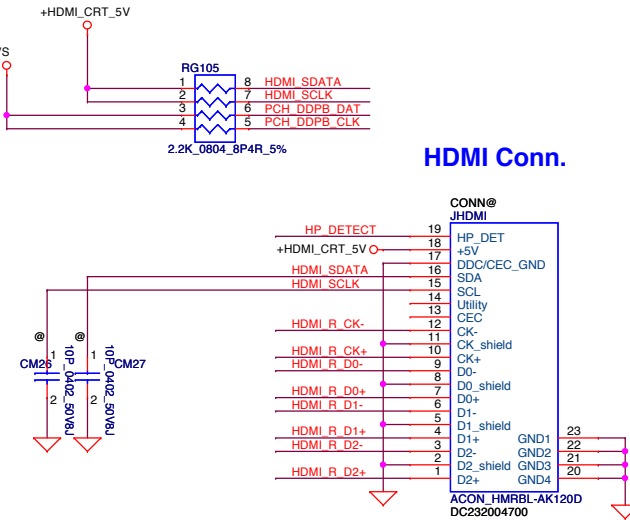
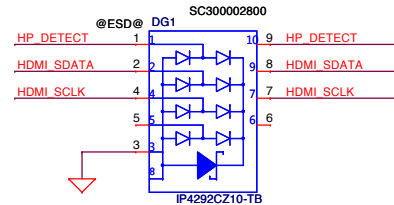
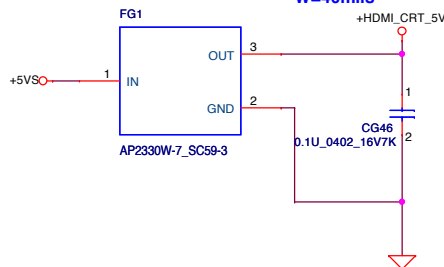
DB phase :
For ESD request
20141117



HDMI Conn.

SI : EMI request to modify HDMI schematic.

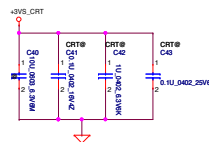
Layout notes
40 mils
W=40mils



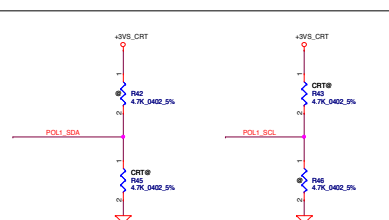
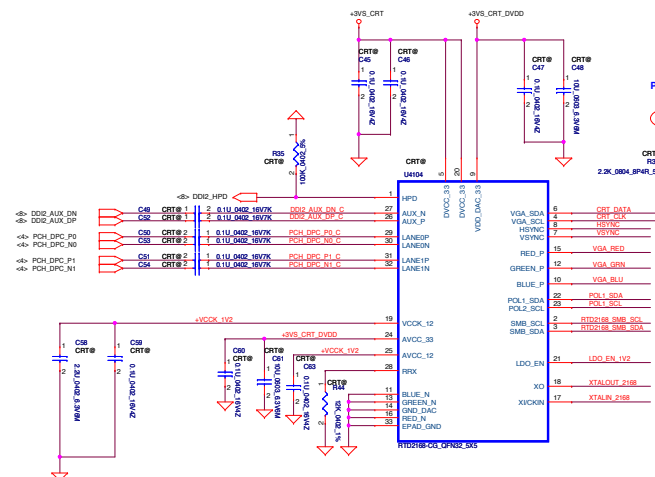
Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	HDMI Conn/Level shift	
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<19,20,23,24,25,26,29,33,37,51,54> +5VS  +5VS
 <12,15,16,18,19,20,22,23,24,25,27,31,32,33,34,35,36,37,56,6,7,8,9> +3VS  +3VS
 <20> +HDMI_CRT_5V  +HDMI_CRT_5V

PV:R34 change to 0-ohm shortpad

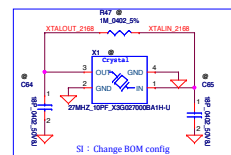


PV:R38 change power for SVTP 3-9.



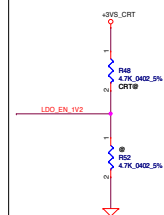
		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high



Select VCCK V12 source from external 1.2V or embedded LDO

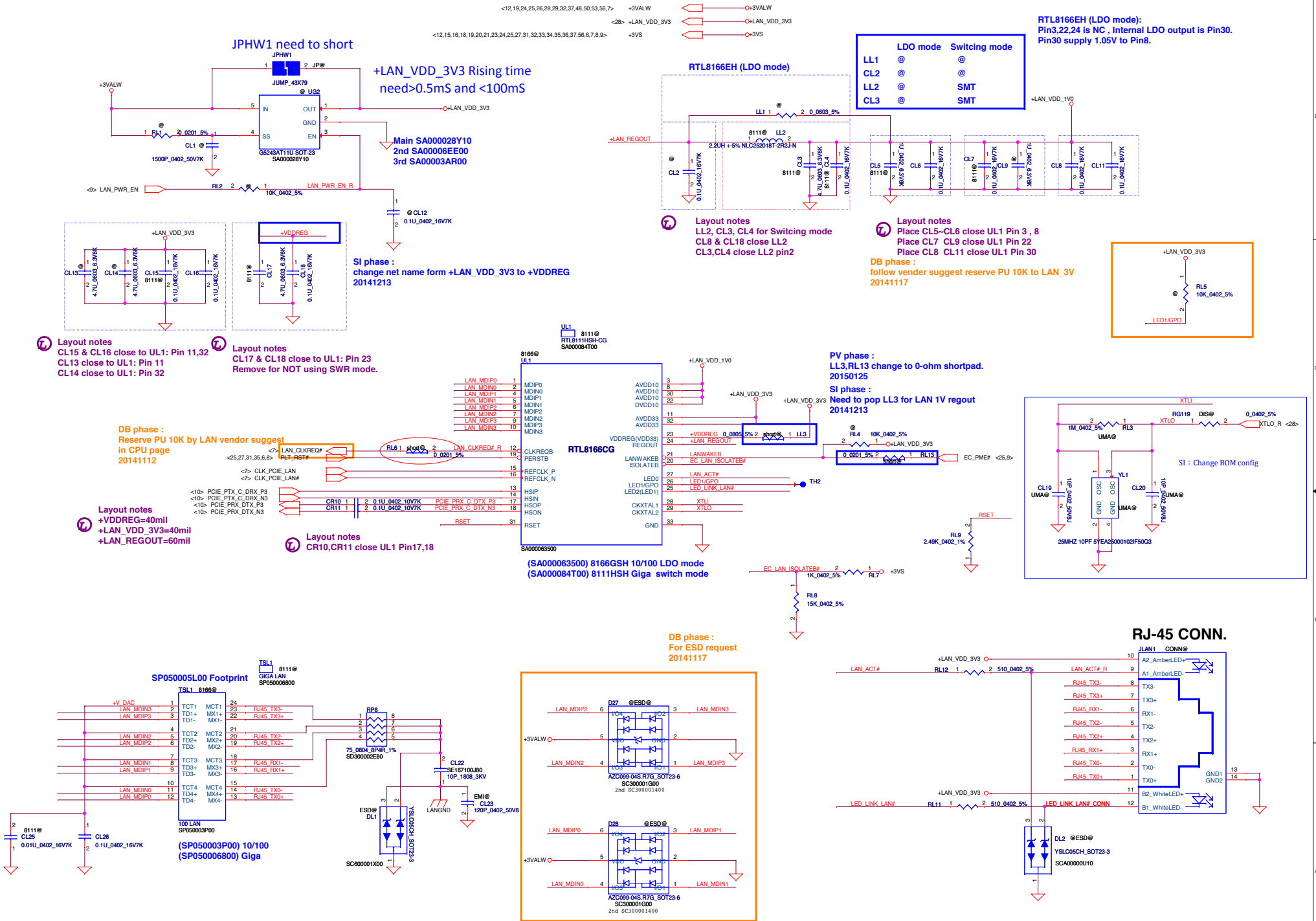
LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO



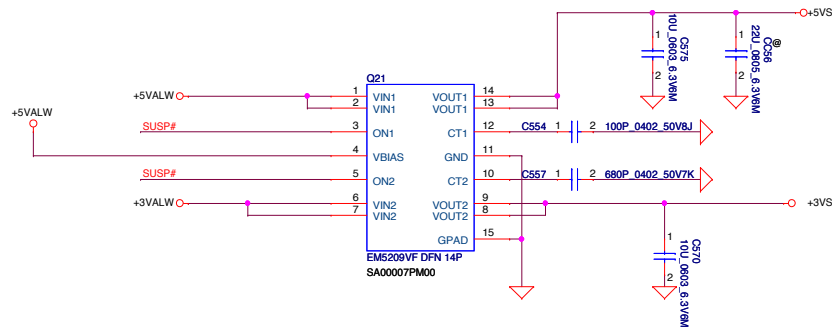
PV:Change L7,L8,L9 value and footprint. 50 impedance

[illegible]

Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.		
Issued Date	2014/02/18	Deciphered Date	2015/02/20	DP to CRT RTD2168		
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			Date	January, 2015	Sheet	21 of 61



+5VALW TO +5VS

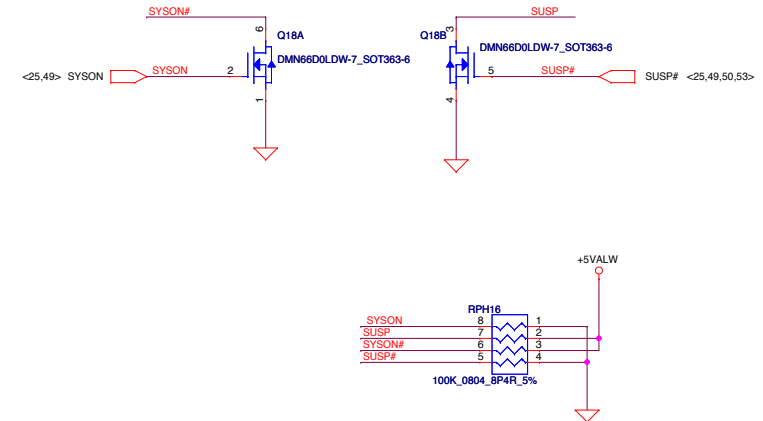
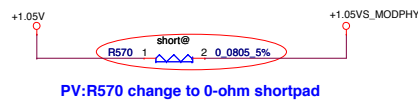


+3VALW TO +3VS

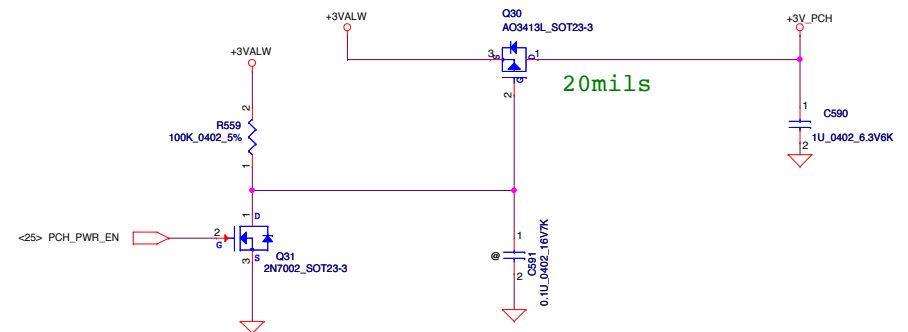
+1.05V TO +1.05VS



+1.05V TO +V1.05DX_MODPHY

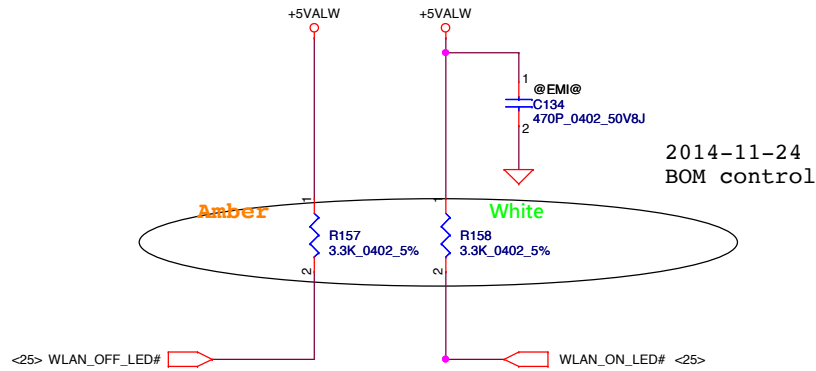
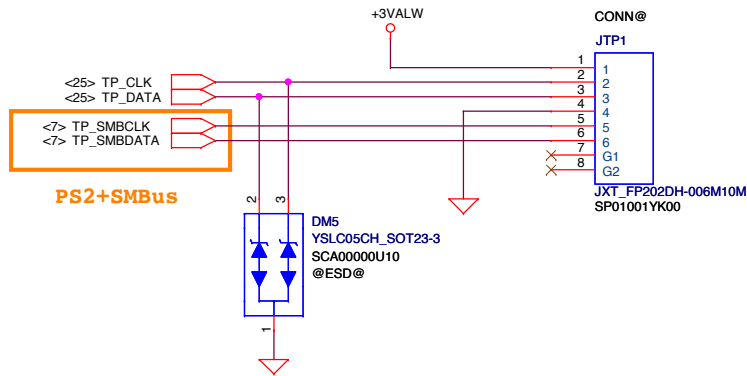


+3VALW TO +3V_PCH

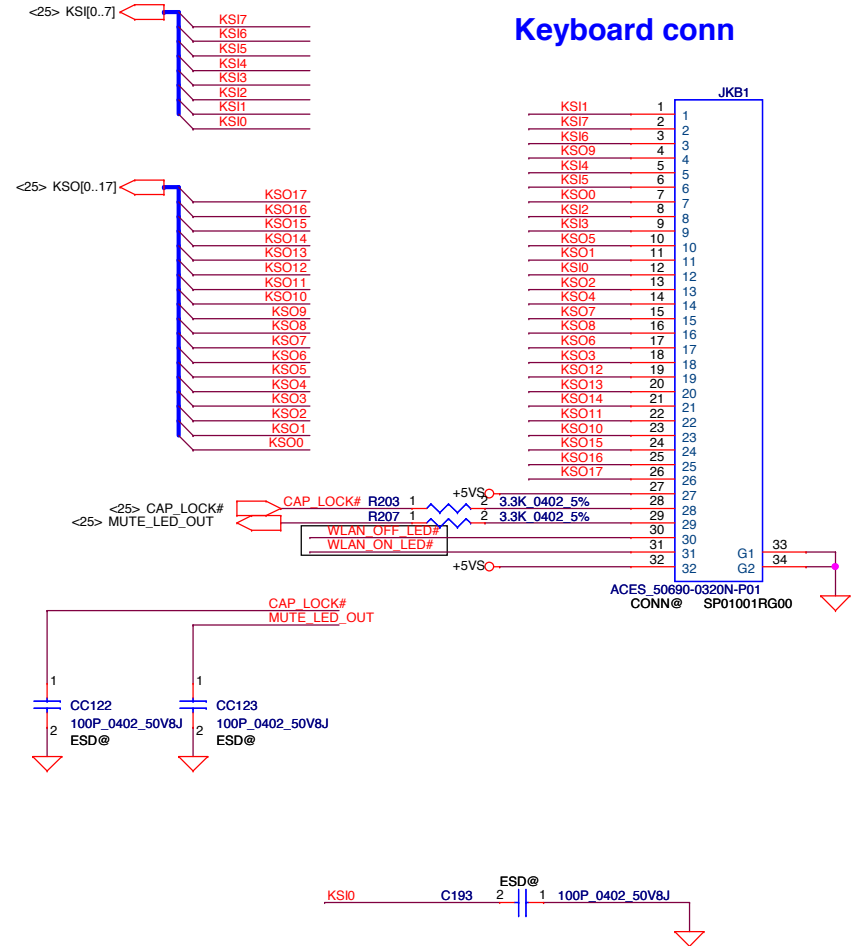


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								DC Interface	
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						Custom		LA-C701P	
						Date:		Saturday, January 31, 2015	
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TP Button BD Connector

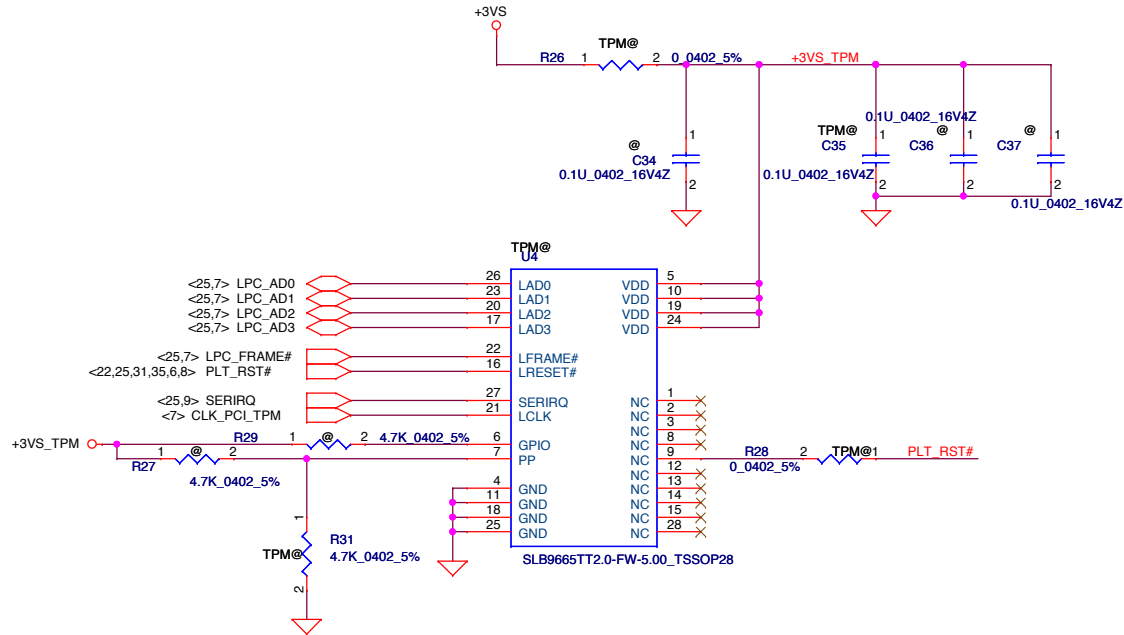


Keyboard conn



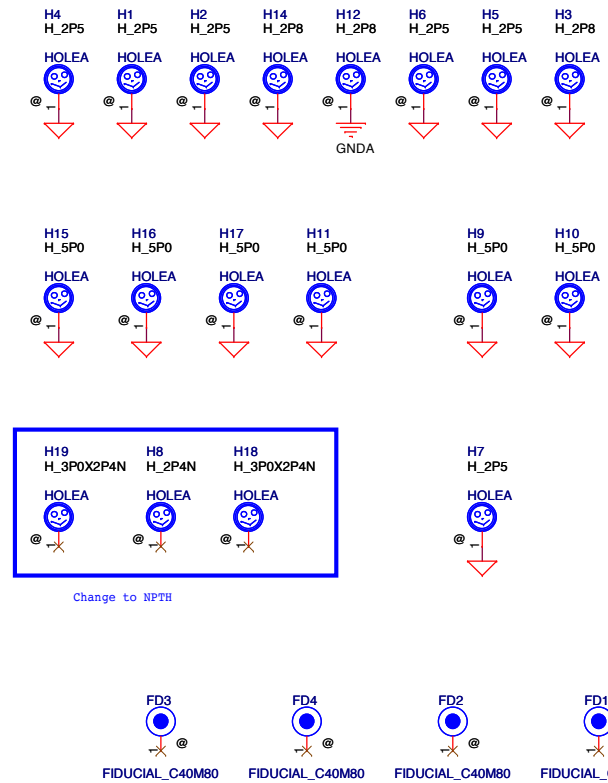
Security Classification		Compal Secret Data				Compal Electronics, Inc.				
Issued Date		2013/02/26		Deciphered Date		2015/07/08		Title		
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TPM2.0



SLB9665 (SA00007XU00)-->TPM2.0
 SLB9660 (SA00007AB00) -->TPM1.2

Screw Hole



Security Classification		Compal Secret Data		Title	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	TPM/Screw	
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				LA-C701P	0.1
Date: Saturday, January 31, 2015				Sheet	61

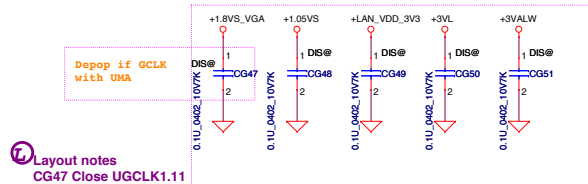
BOM control

Platform	Silego P/N	Compal PN	25MHz(A)	32.768KHz	24MHz(B)	27MHz	8MHz	Remark
Intel ULT UMA	SLG3NB3455VTR	SA00008IQ00	1	1	1	X	X	@
Intel ULT Dis	SLG3NB3456VTR	SA00008J800	1	1	1	1	X	DIS@

Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X'TAL use 10ppm.

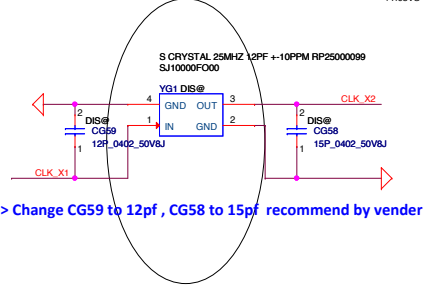
<36,37,38,56>	+1.8VS_VGA	○+1.8VS_VGA
<11,12,24,25,34,37,50,51>	+1.05VS	○+1.05VS
<22>	+LAN_VDD_3V3	○+LAN_VDD_3V3
<25,32,46,47,48,6>	+3VL	○+3VL
<12,19,22,24,25,26,29,32,37,48,50,53,56,7>	+3VALW	○+3VALW
<8>	+RTCBATT	○+RTCBATT
<12,6,8>	+RTCVCC	○+RTCVCC

- 20141120 vendor recommend
1. AMD GPU power rail should be 1.8V, please modify +3VS_VGA to AMD GPU power rail.
 2. CG47, CG48, CG49, CG50 and CG51 must placed close to UGCLK1.11, UGCLK1.13, UGCLK1.8, UGCLK1.15 and UGCLK1.2.
 3. Please place RG114, RG109, RG111 and RG113 close to UGCLK1 for impedance matching.
 4. Modify RG114 Symbol from 8 to UGCLK1.
 5. Change RG109 value from 33ohm to 10ohm.
 6. We recommend to add RGxxx and R0yyy for isolated 32.768k and 24M clock tail.
 7. We recommend to add CGxxx, it is reserved for BML.
 8. We recommend to change CG54 Symbol from GCLK# to 8.

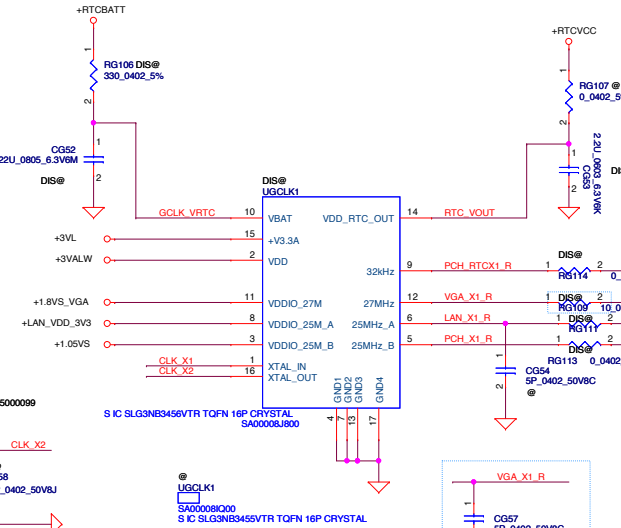


- Layout notes
- CG47 Close UGCLK1.11
 - CG48 Close UGCLK1.13
 - CG49 Close UGCLK1.8
 - CG50 Close UGCLK1.15
 - CG41 Close UGCLK1.2

SI phase 20141225
Change YG1 PN to SJ10000F000



<SI> Change CG59 to 12pf, CG58 to 15pf recommend by vender



Layout notes

Please place RG114, RG109, RG111 and RG113 close to UGCLK1 for Impedance matching.

Change RG109 to 10 ohm recommend by vender

- 20141120 add RG115 RG116 isolated GreenCLK tail from vendor suggest

<CPU> YC1 P6

<GPU> Y6 P37

<LAN> YL1 P22

<CPU> YC2 P7

Layout notes

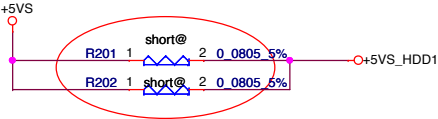
For isolated GreenCLK tail
RG110 close to Y6 (27M for GPU)
RG112 close to YL1 (25M for LAN)
RG115 close to YC1 (32.768k for CPU)
RG116 close to YC2 (24M for CPU)

Layout notes

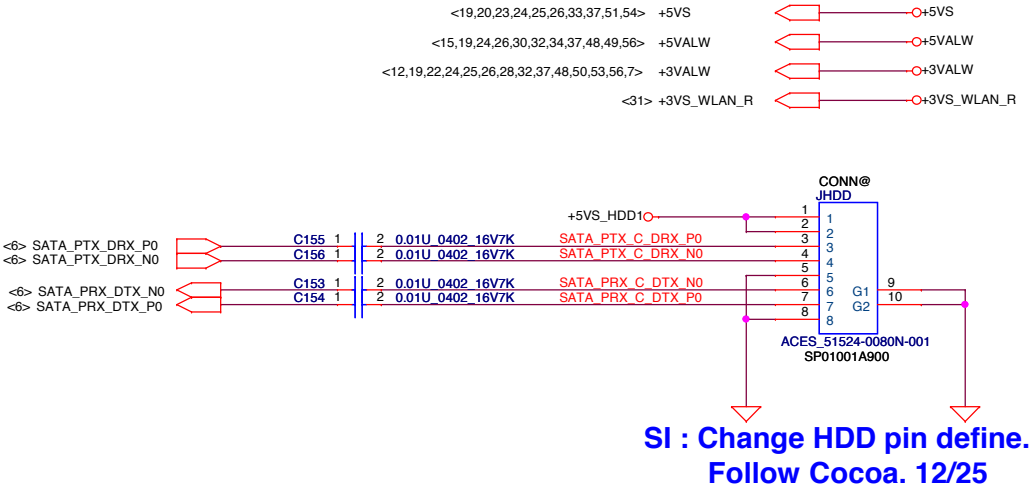
Place CG57 between UGCLK1 and RG109
Reserve CG55 for vendor Place between UGCLK1 and RG113

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Issued Date	2013/06/10	Deciphered Date	2014/07/01
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		Sheet	26 of 61
		Rev	0.1

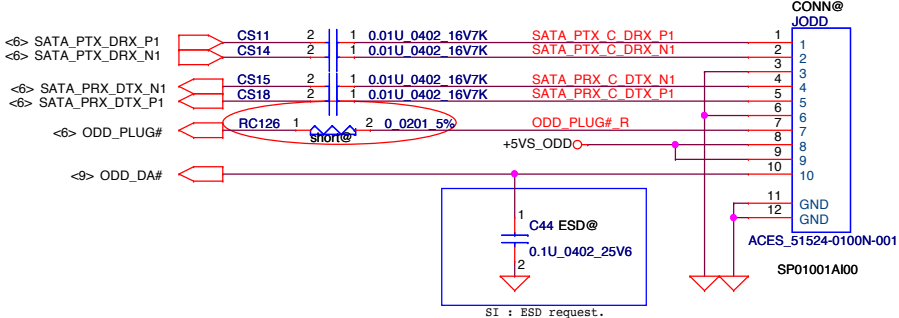
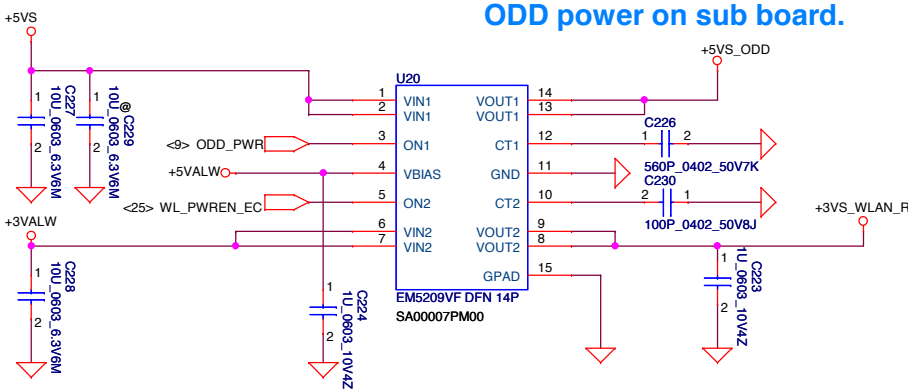
2.5" SATA HDD



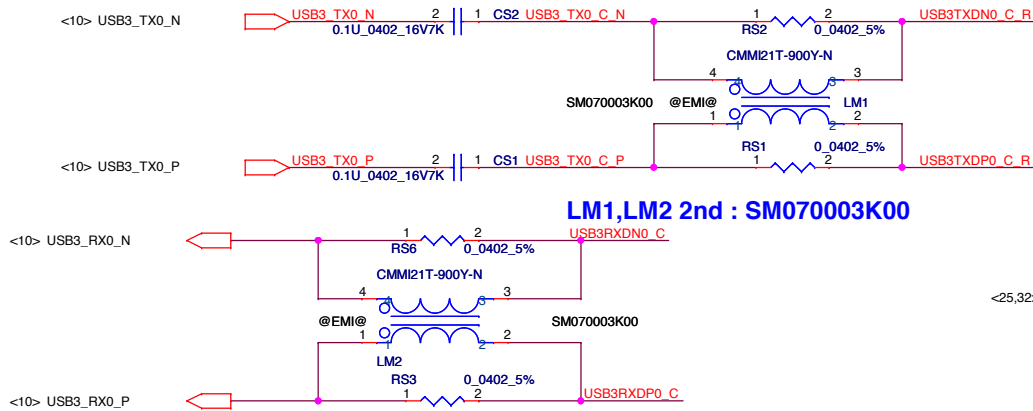
HDD power on sub board.
PV : Change R201,R202 to 0-ohm shortpad.
20150125



2.5" SATA ODD

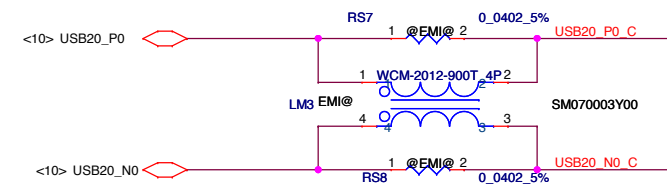


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								Size	Document Number			Rev			
								B	LA-C701P			0.1			
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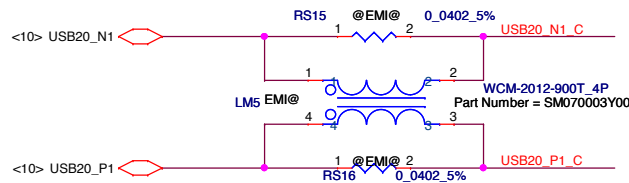


LM1,LM2 2nd : SM070003K00

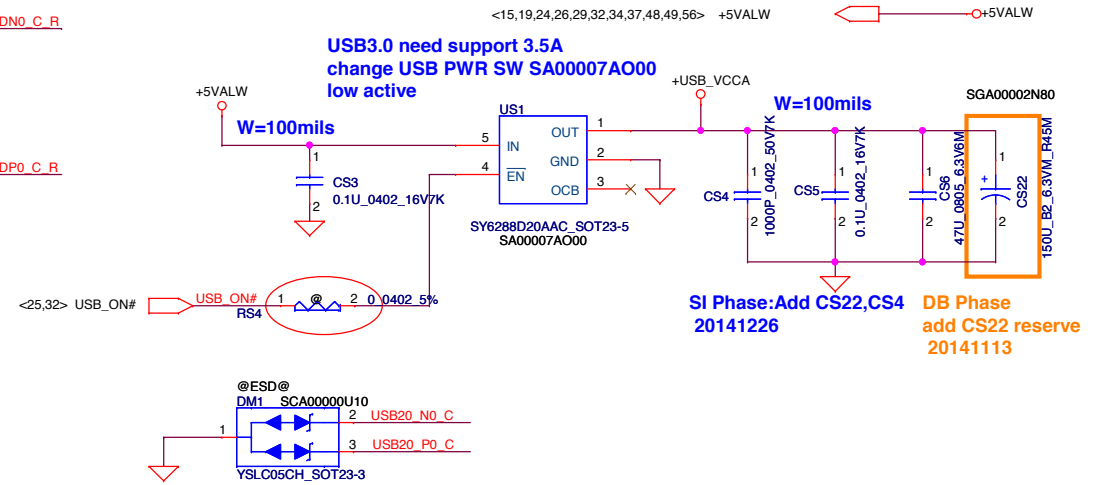
LM3 2nd : SM070002J00



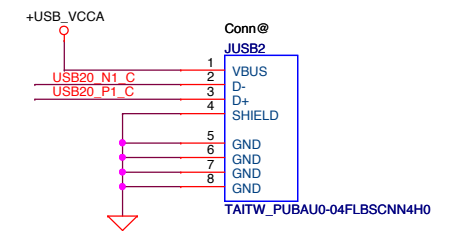
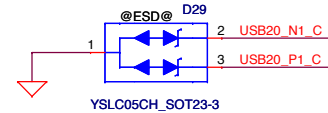
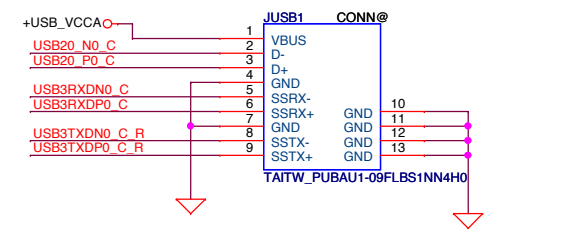
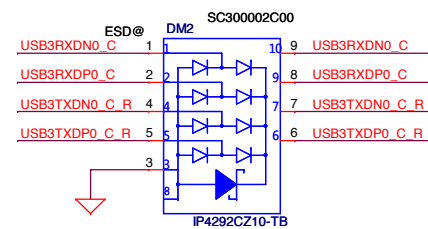
USB2.0 port x 1



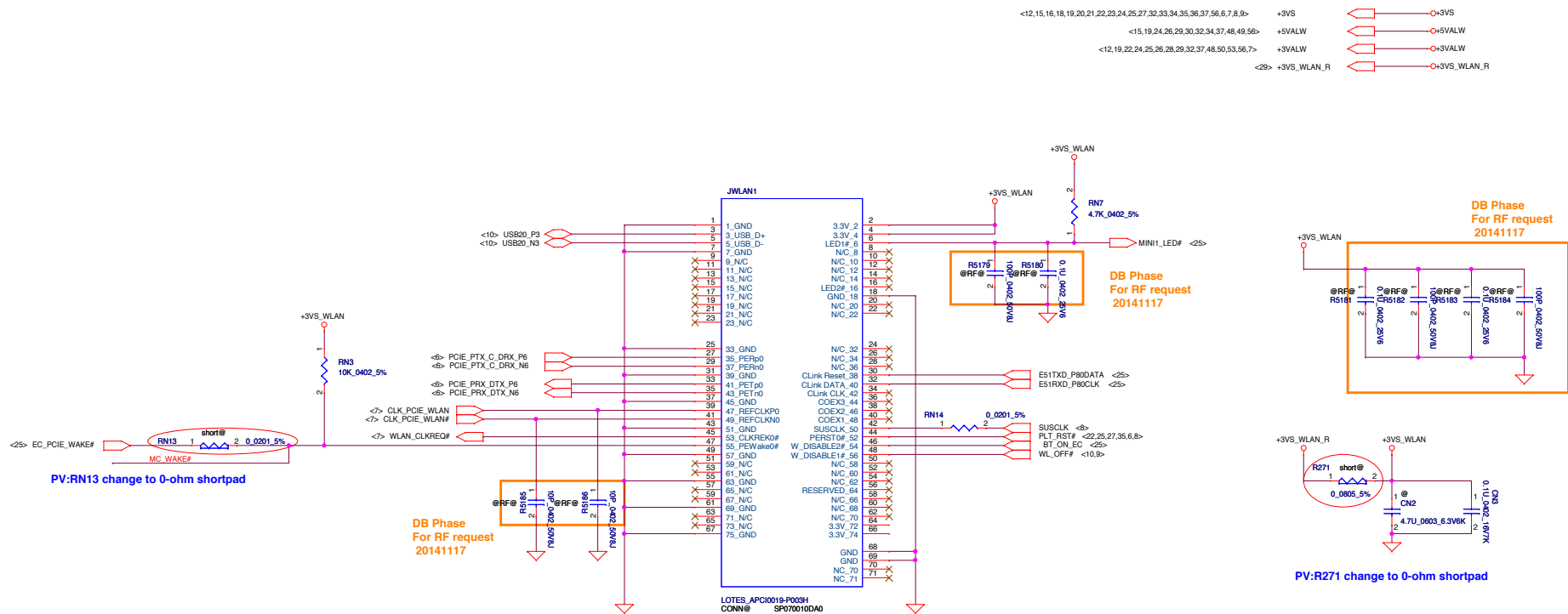
LM5 2nd : SM070002J00



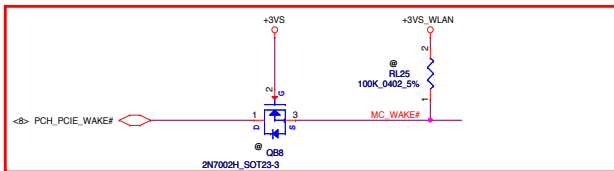
SI : pop DM2.



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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	USB 3.0/2.0 conn
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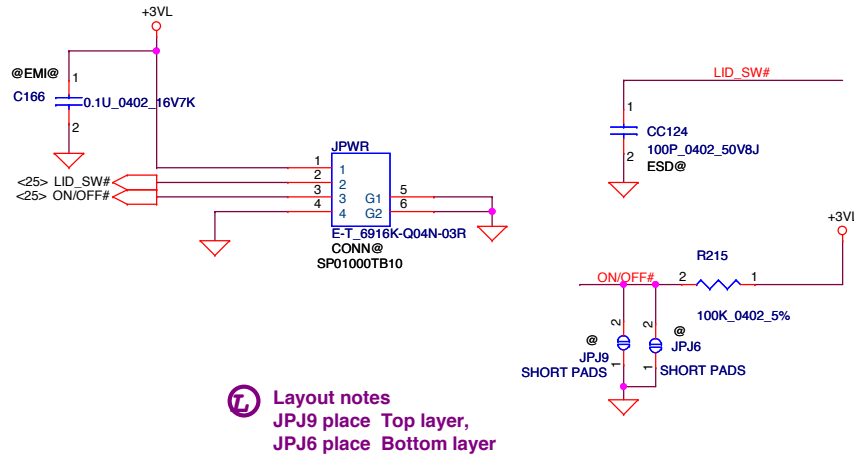
NGFF and WLAN



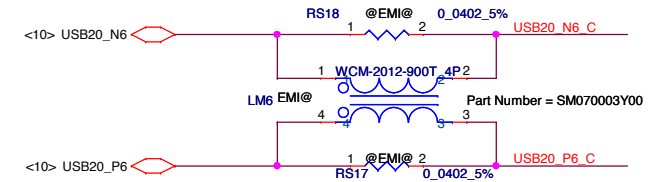
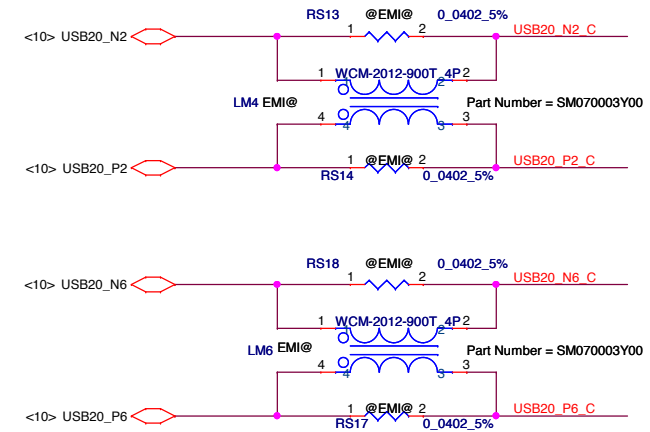
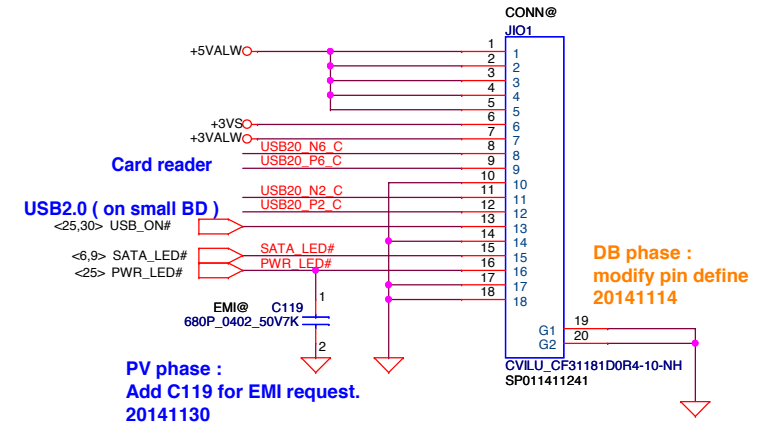
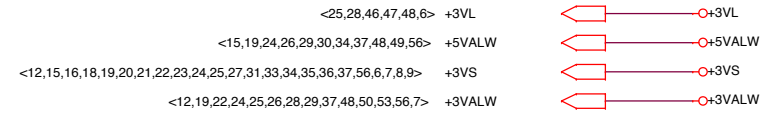
Unpop QB4 and RL23 for not support OBFF

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				Size Document Number
				LA-C701P
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				0.1
				Date: Saturday, January 31, 2015
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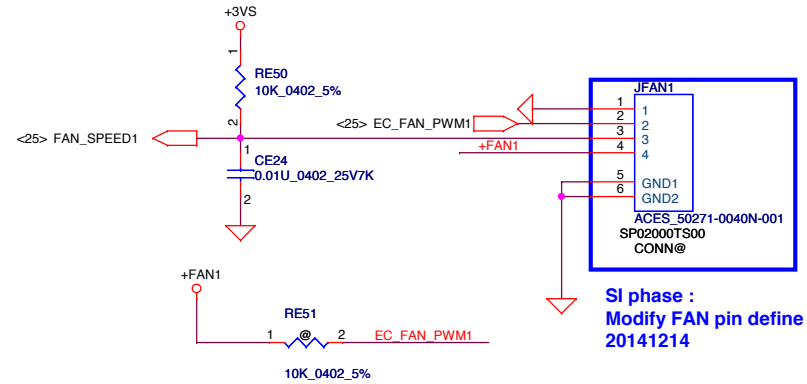
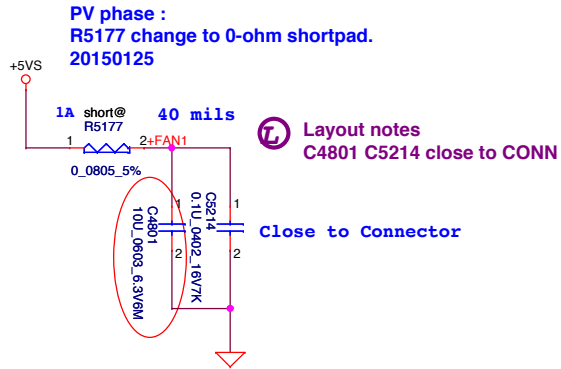
Power Button Connector



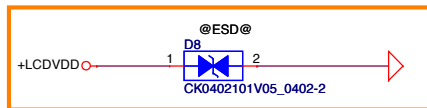
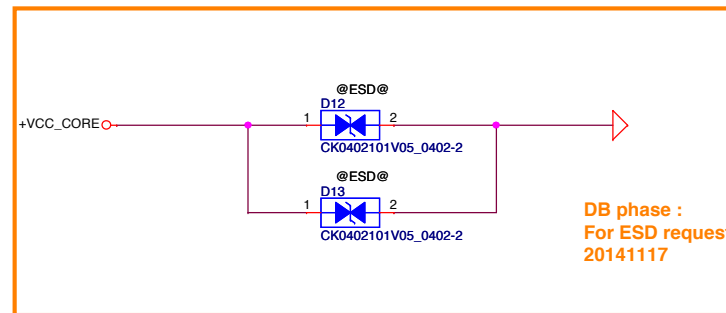
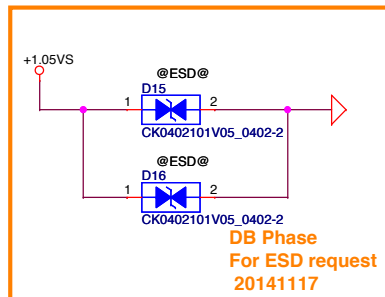
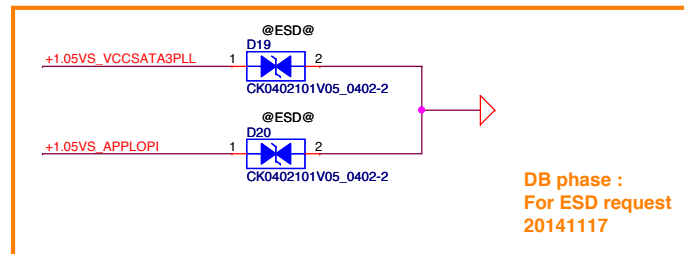
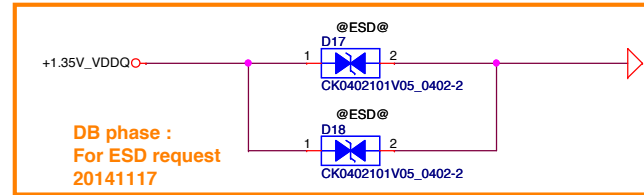
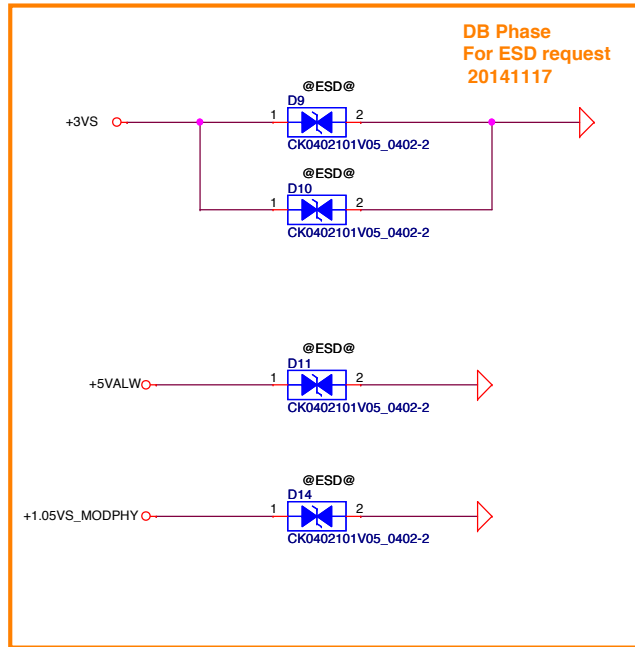
IO BD Connector (USB2.0,Card reader,HDD & PWR LED) 11/26 change CONN.



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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	IO CON
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				Date:	Saturday, January 31, 2015
				Sheet	32 of 61

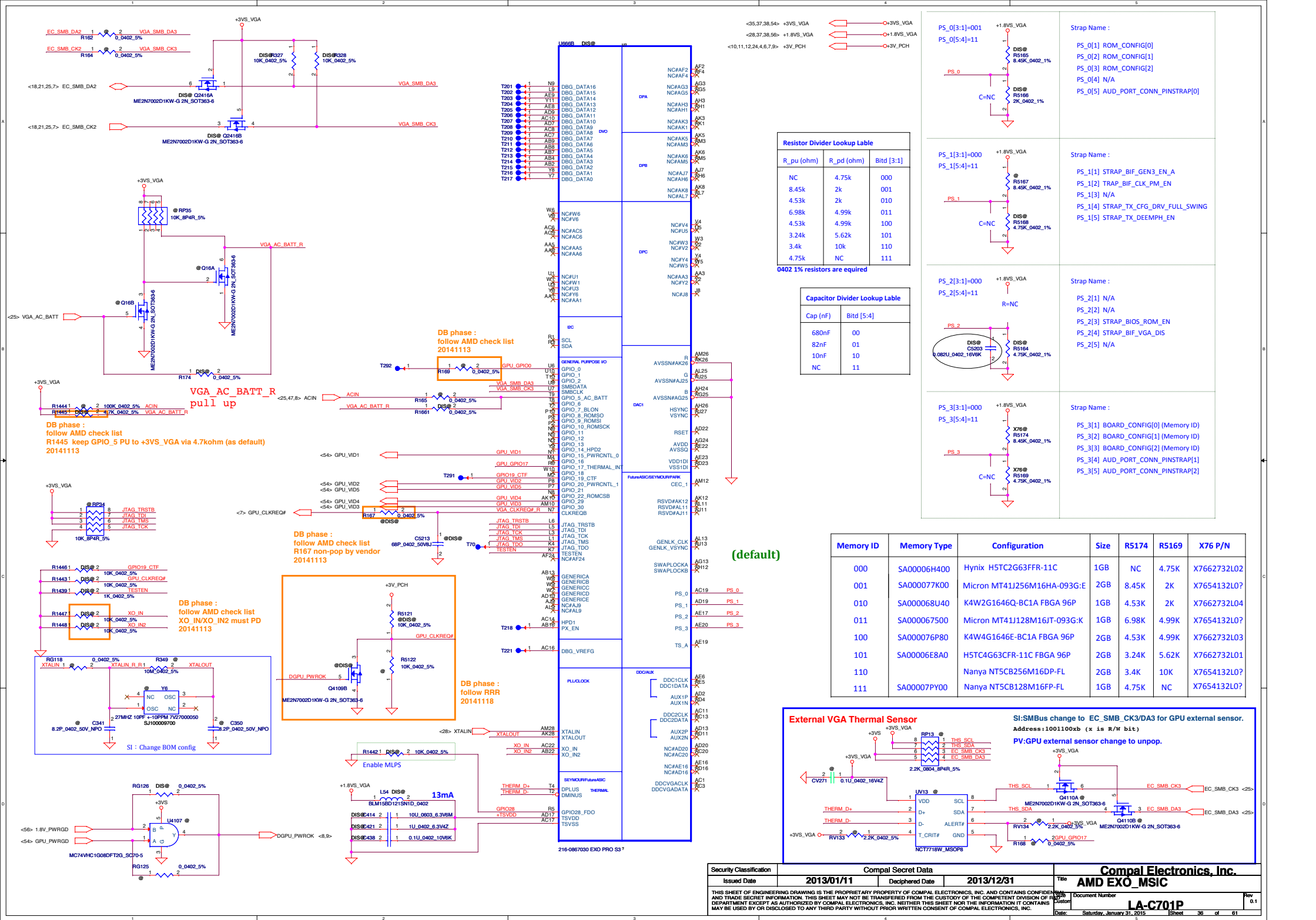


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				Date:	Saturday, January 31, 2015
				Sheet	33 of 61

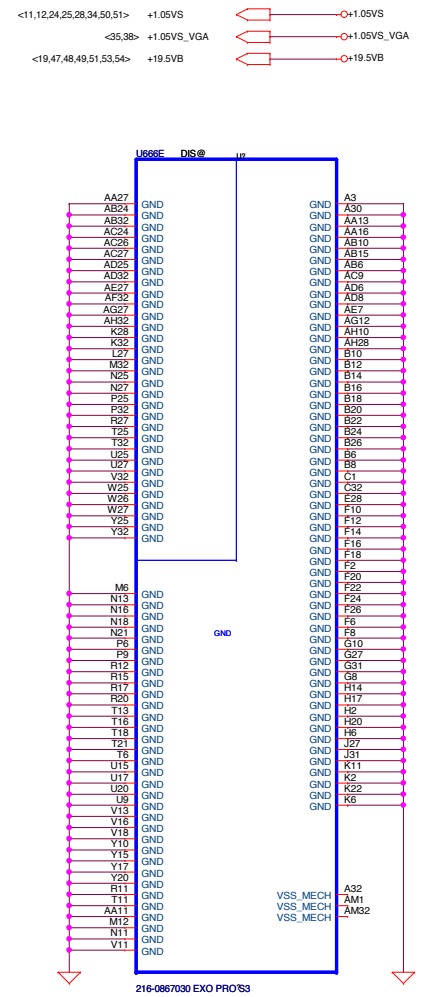
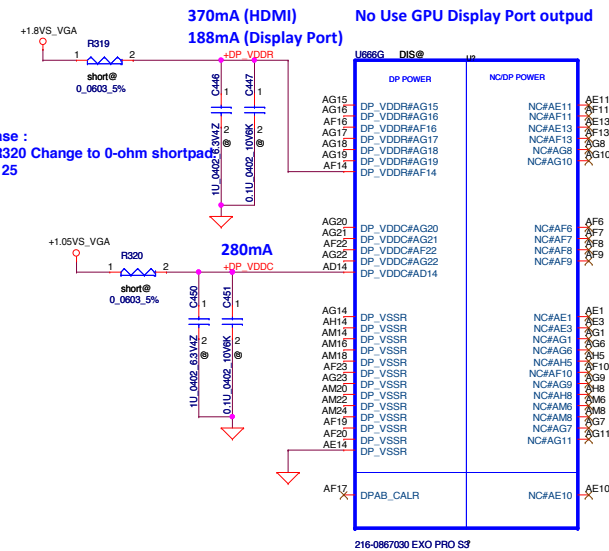


<12,15,16,18,19,20,21,22,23,24,25,27,31,32,33,35,36,37,56,6,7,8,9>	+3VS		+3VS
<15,19,24,26,29,30,32,37,48,49,56>	+5VALW		+5VALW
<12,24>	+1.05VS_MODPHY		+1.05VS_MODPHY
<11,12,24,25,28,37,50,51>	+1.05VS		+1.05VS
<18,19>	+LCDVDD		+LCDVDD
<11,15,16,17,4,49>	+1.35V_VDDQ		+1.35V_VDDQ
<12,6>	+1.05VS_VCCSATA3PLL		+1.05VS_VCCSATA3PLL
<12>	+1.05VS_APPLOPI		+1.05VS_APPLOPI

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					LA-C701P	0.1
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<15,19,24,26,29,30,32,34,48,49,56>	+5VALW		+5VALW
<38,54,55>	+VGA_CORE		+VGA_CORE
<19,20,23,24,25,26,29,33,51,54>	+5VS		+5VS
<3,22,24,25,26,28,29,32,48,50,53,56,7>	+3VALW		+3VALW



AMD feedback :
Exo ASIC normally is 0.95v ,
can support to 1.05v functionally.



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2013/01/11	Deciphered Date	2013/02/31	Title	AMD EXO Power/GND	
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				Custom	LA-C701P	0.1
				Date:	Saturday, January 31, 2015	Sheet 37 of 61

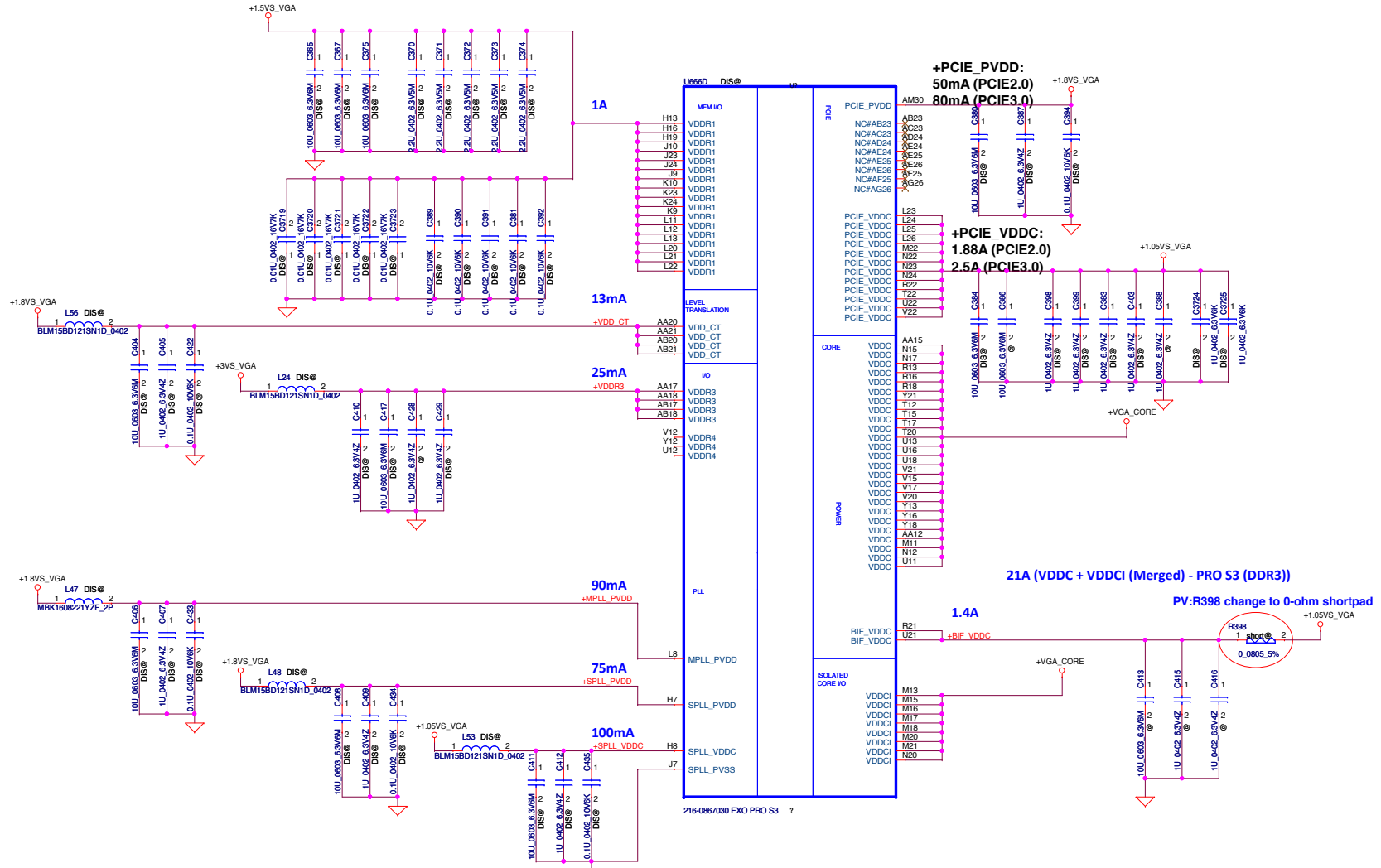
+VGA_CORE	10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)
VDDCI	3.5A	1	3

+0.95VS_VGA	10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)
BIF_VDDC	1.4A	0	0
SPLL_VDDC	100mA	1	1

+1.5VS_VGA	10uF	1uF	0.1uF
VDDR1	1.5A	3	5

+1.8VS_VGA	10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1
MPLL_PVDD	130mA	1	1
SPLL_PVDD	75mA	1	1
VDDR4	(300mA)	0	0
VDD_CT	13mA	1	1
+TSVDD	13mA	1	1
+DP_VDDR	0	0	0
+DP_VDDC	0	0	0

+3VS_VGA	10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)

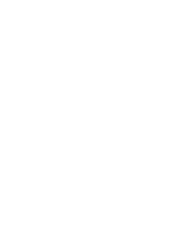
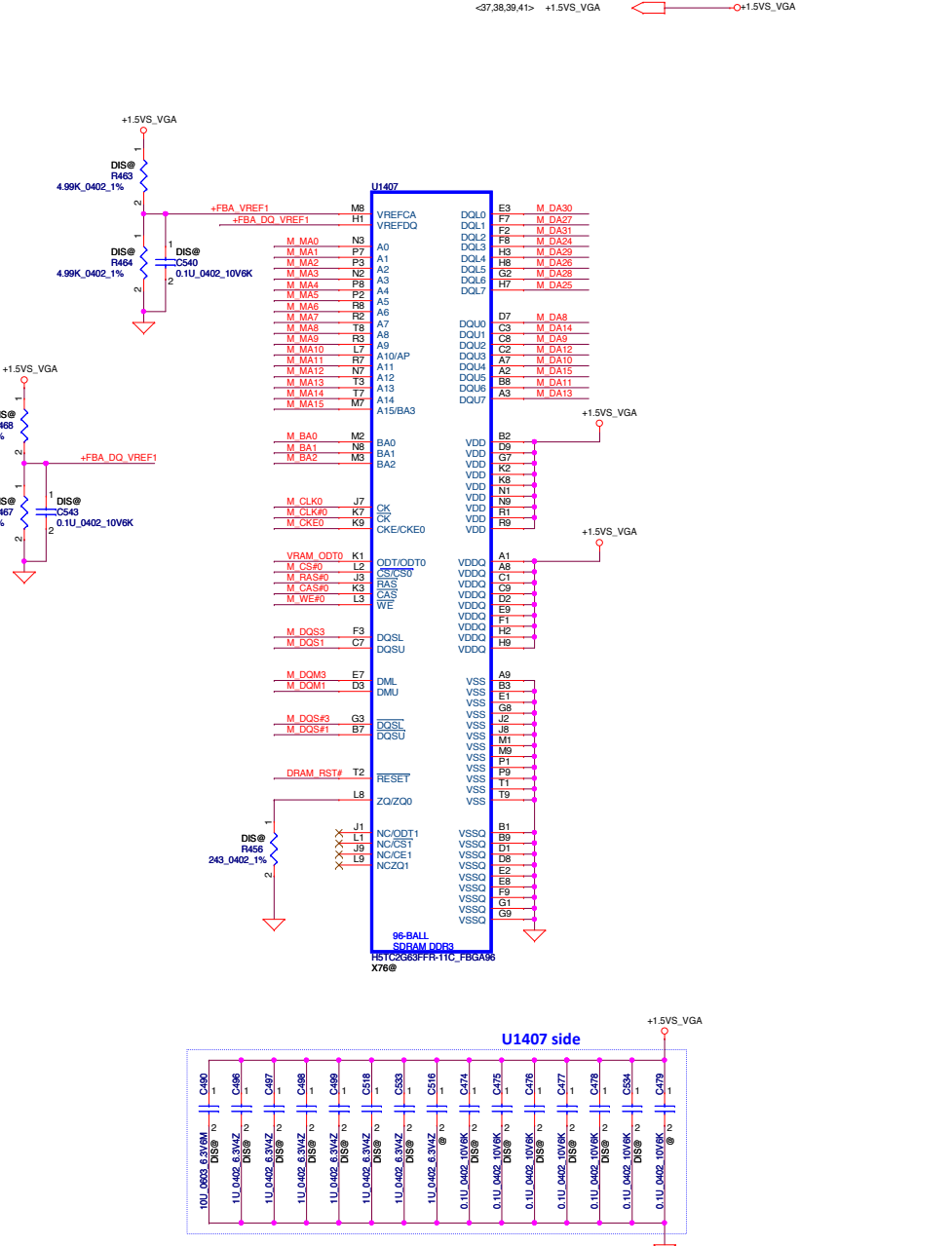
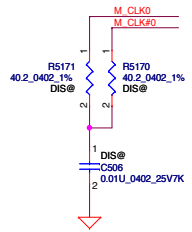
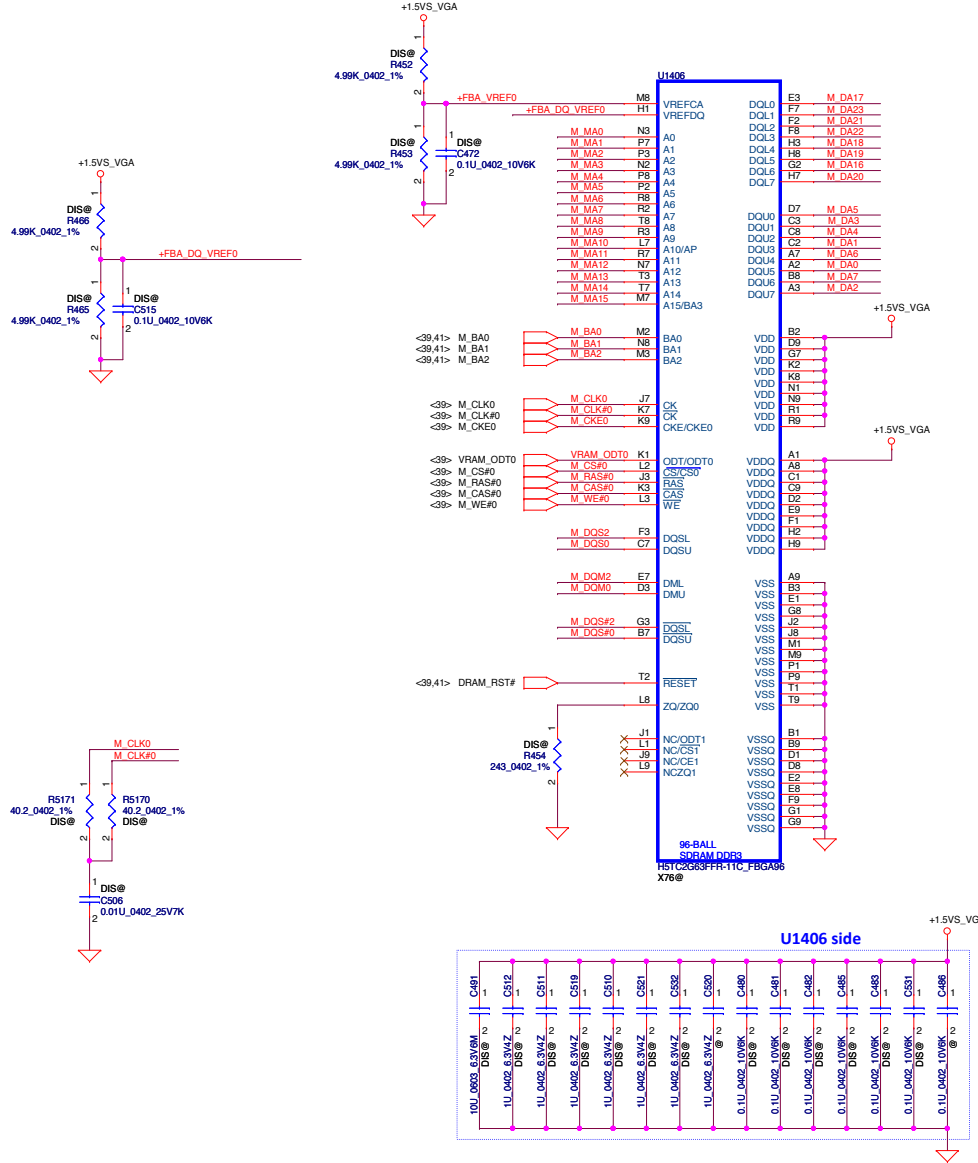




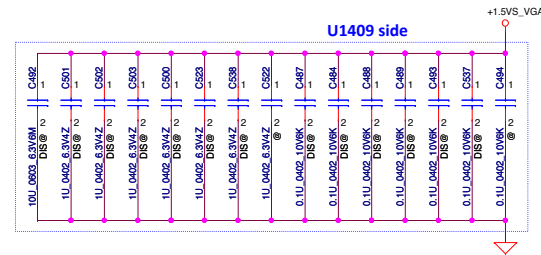
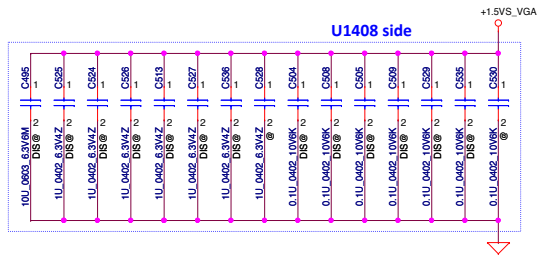
Size Custom	Document Number LA-C701P	Rev 0.1
Date: Saturday, January 31, 2015	Sheet 39 of 61	

Memory Partition A - Lower 32 bits

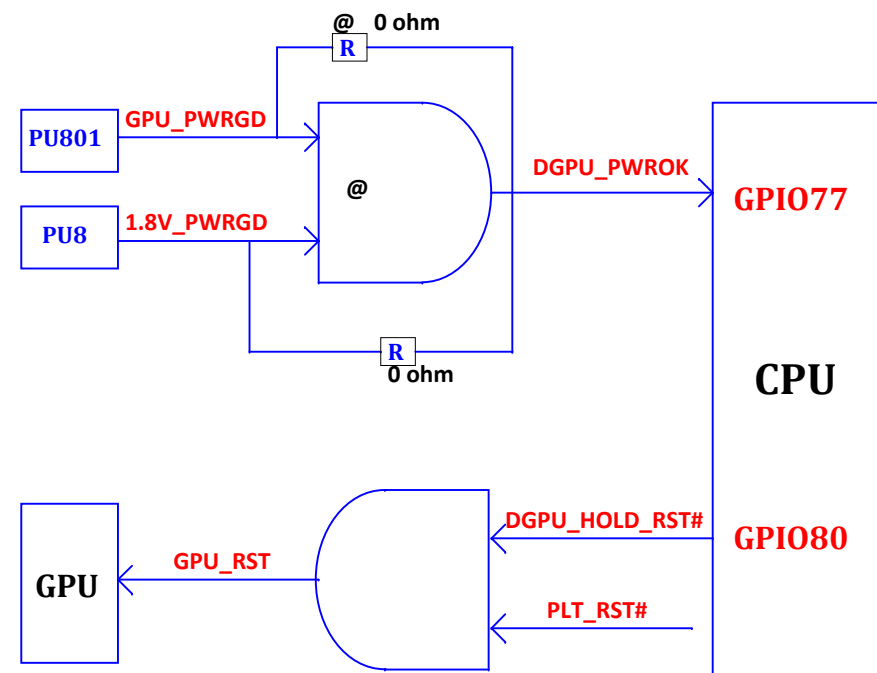
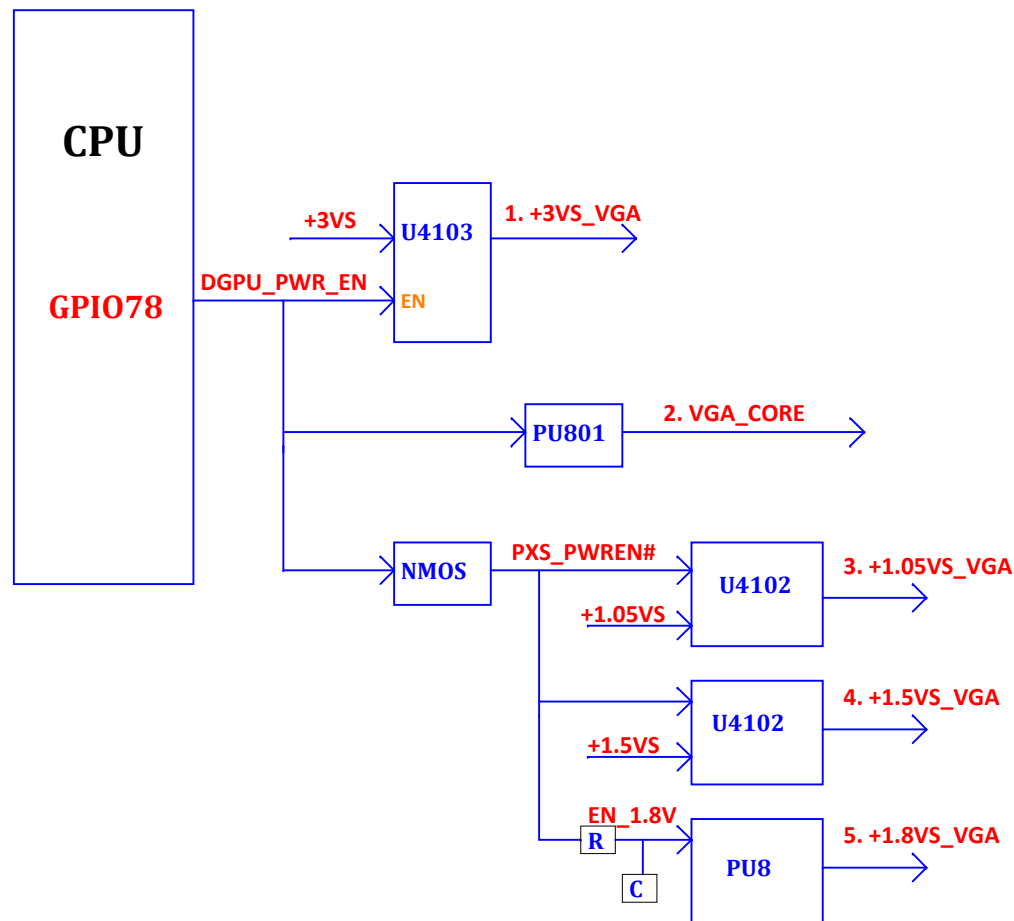
- <39,41> M_DA[63..0] M_DA[63..0]
- <39,41> M_MA[15..0] M_MA[15..0]
- <39,41> M_DQM[7..0] M_DQM[7..0]
- <39,41> M_DQS[7..0] M_DQS[7..0]
- <39,41> M_DQS[7..0] M_DQS[7..0]

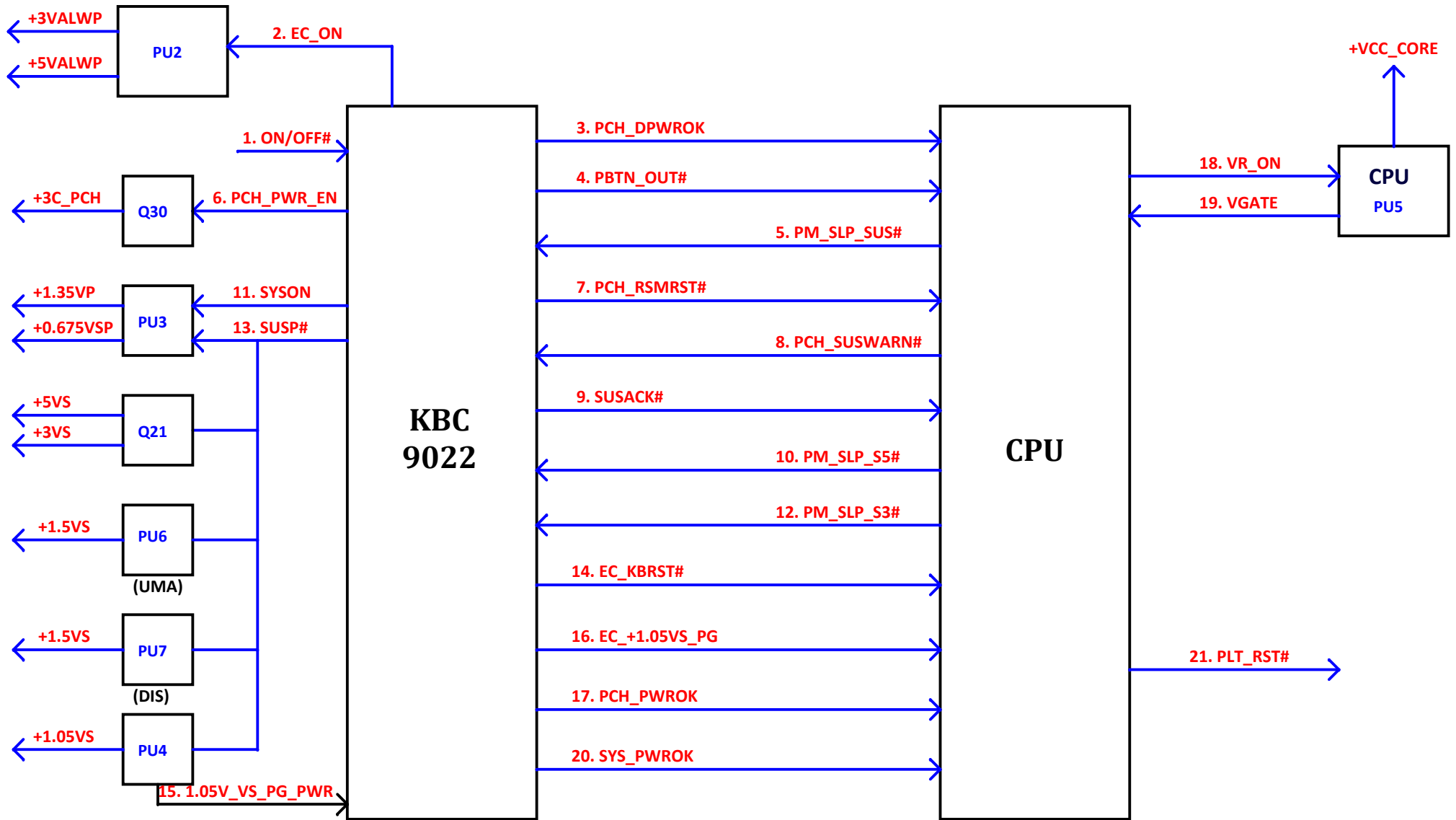


<39,40>	M_DA[63..0]		M_DA[63..0]
<39,40>	M_MA[15..0]		M_MA[15..0]
<39,40>	M_DQM[7..0]		M_DQM[7..0]
<39,40>	M_DQS[7..0]		M_DQS[7..0]
<39,40>	M_DQS#[7..0]		M_DQS#[7..0]



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				Size		Document Number		Rev 0.1	
				Custom		LA-C701P			
Date:				Saturday, January 31, 2015		Sheet 41 of 61			





Vinafix.com

DB build CPU type

UCPU1



i7-5500U BDW
SA000089A00

UCPU1



i3-5005U BDW
SA000083E50

UCPU1



i3 4005U
SA000072Q80

ZZZ004



HY1@
1G Hynix
X7662732L02

ZZZ004



HY2@
2G Hynix
X7662732L01

ZZZ



DAX

DA6001DO000

ZZZ004



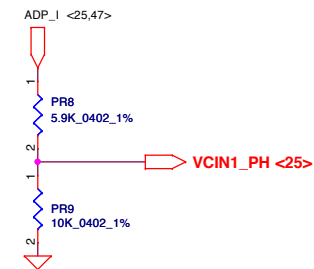
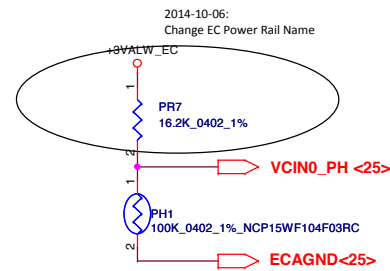
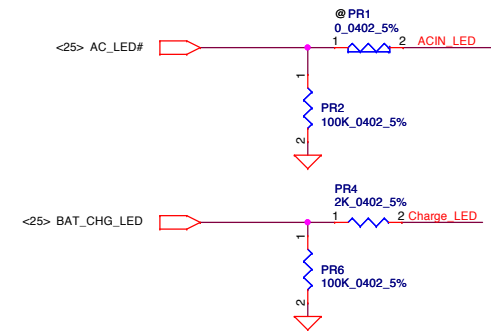
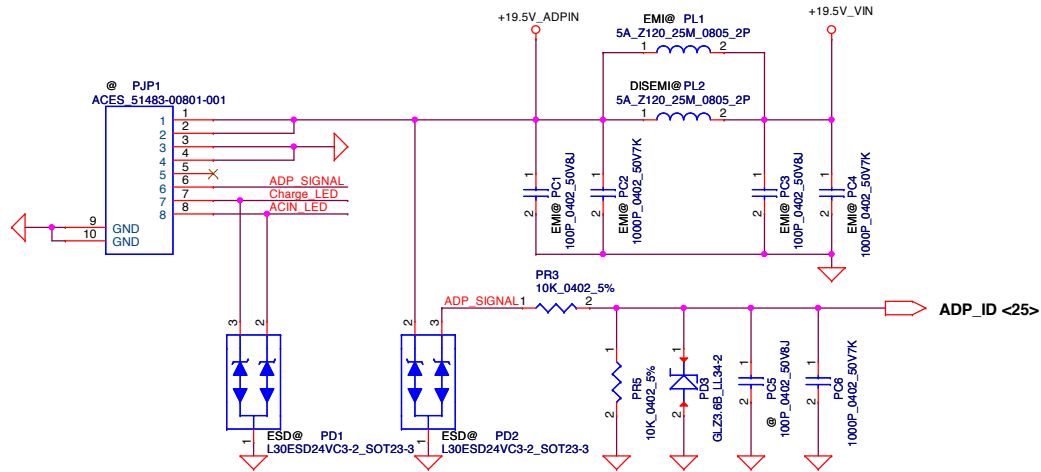
SAM2@
2G SAMSUNG
X7662732L03

ZZZ004

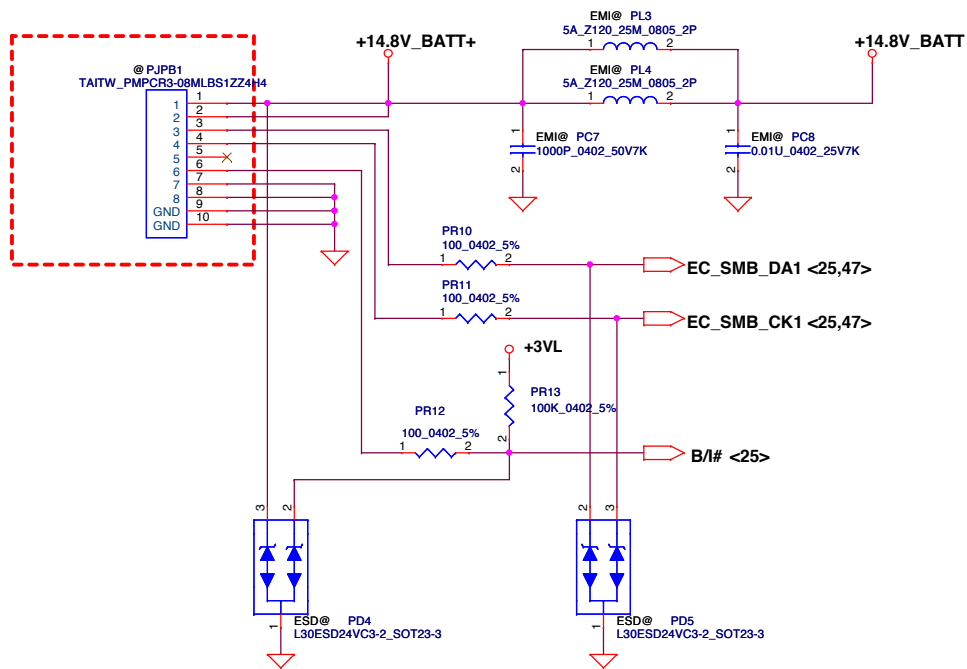


SAM1@
1G SAMSUNG
X7662732L04

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				Date:	Saturday, January 31, 2015	Sheet 44 of 61
				LA-C701P		0.1

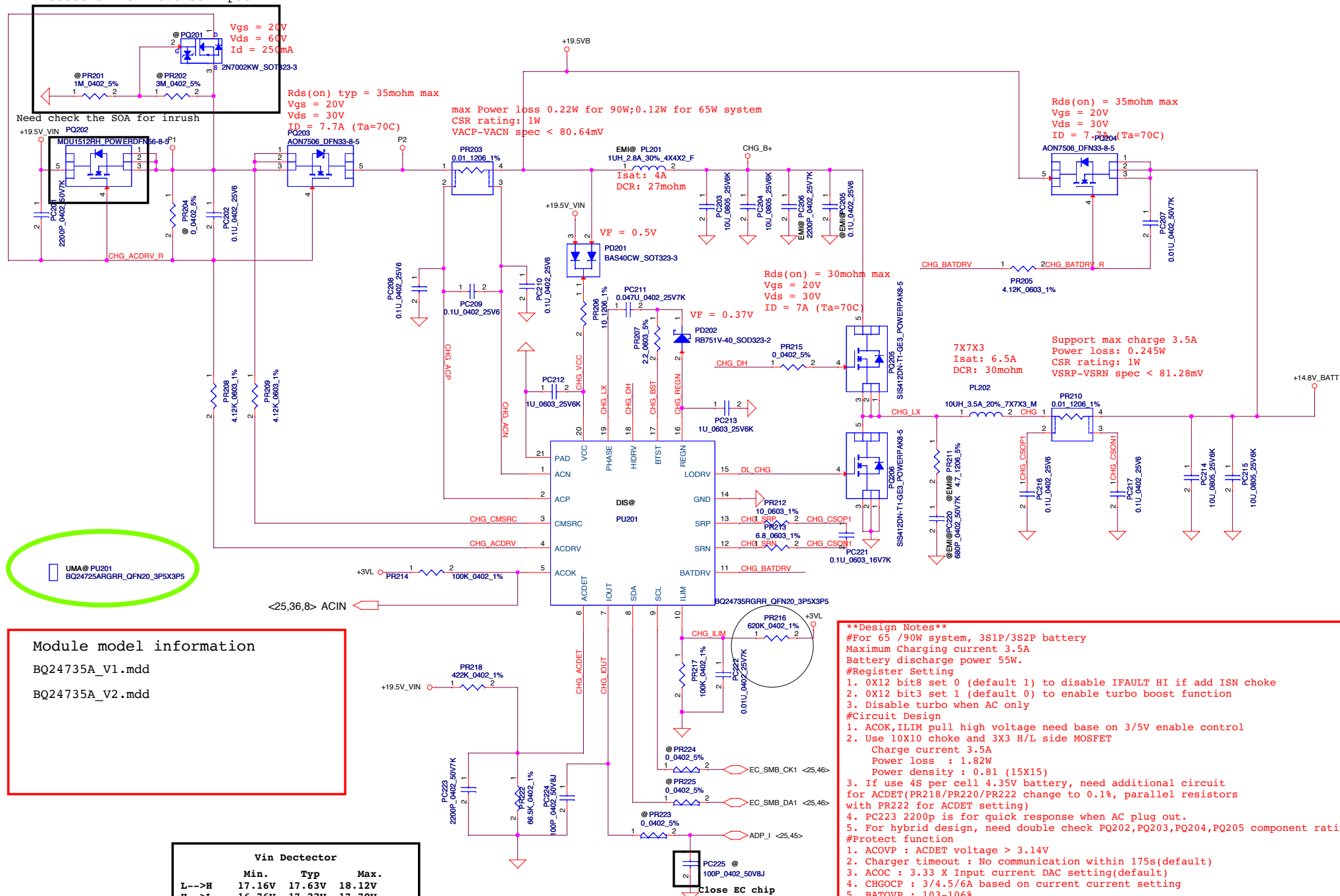


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				Sheet	46 of 60
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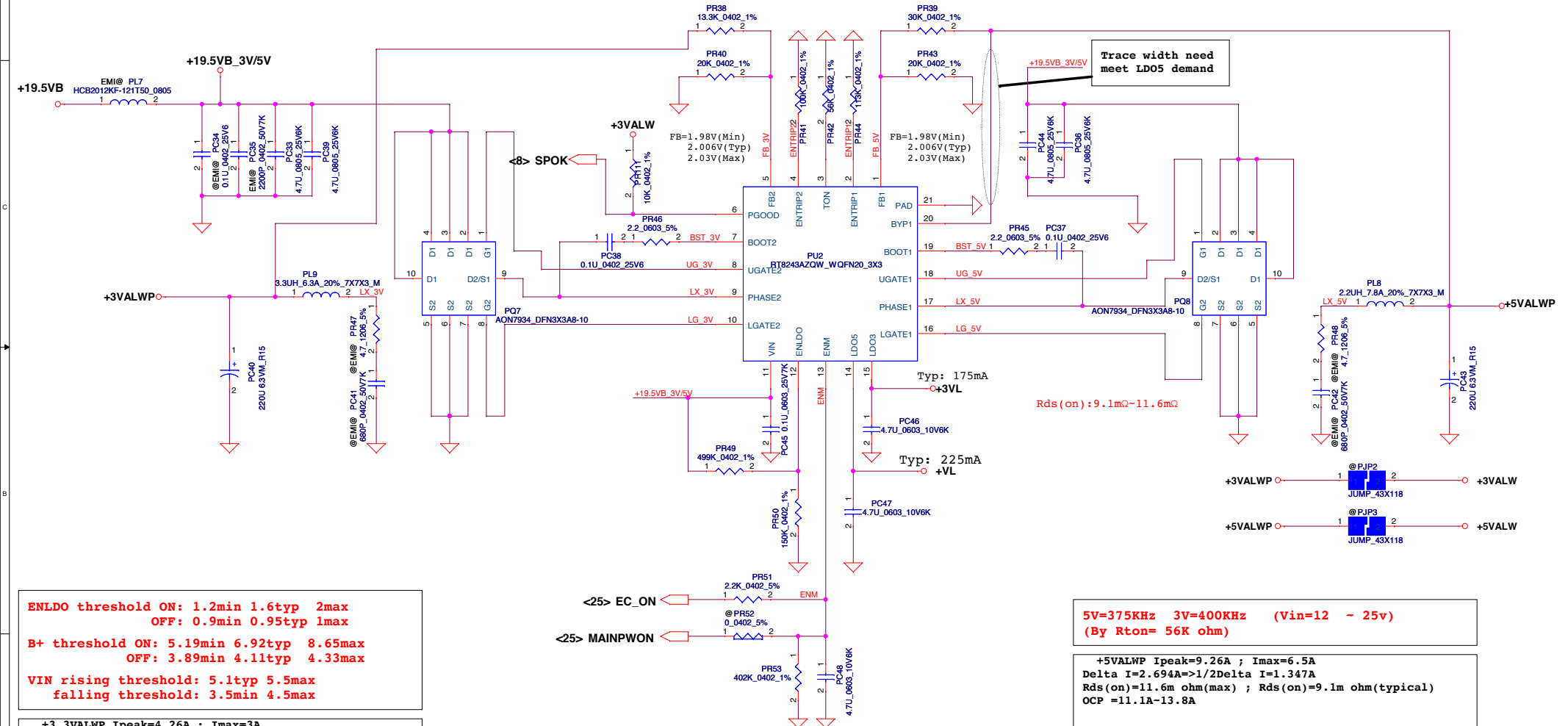
Protection for reverse input



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2014/07/02				PWR-CHARGER			
Deciphered Date				2012/07/02				Common Circuit			
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RT8243A_V1.mdd

ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LDO5	LDO3	+5VALW	+3VALW
Low	Low	X	X	Off	Off	Off	Off
">1.6V" =>High	Low	X	X	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	Off	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	On	On	On	Off	On
">1.6V" =>High	">2.3V" =>High	On	On	On	On	On	On
">1.6V" =>High	">2.3V" =>High	On	Off	On	On	On	Off



TDC:4.9A Fsw:321KHz
H-MOS PD:0.4173W ΔT :13.4°C
L-MOS PD:0.3442W ΔT :10°C
Choke PD:1.9613W ΔT :30°C
OVP margin for Vos:9% @ 330uF cap, 8% @ 220uF

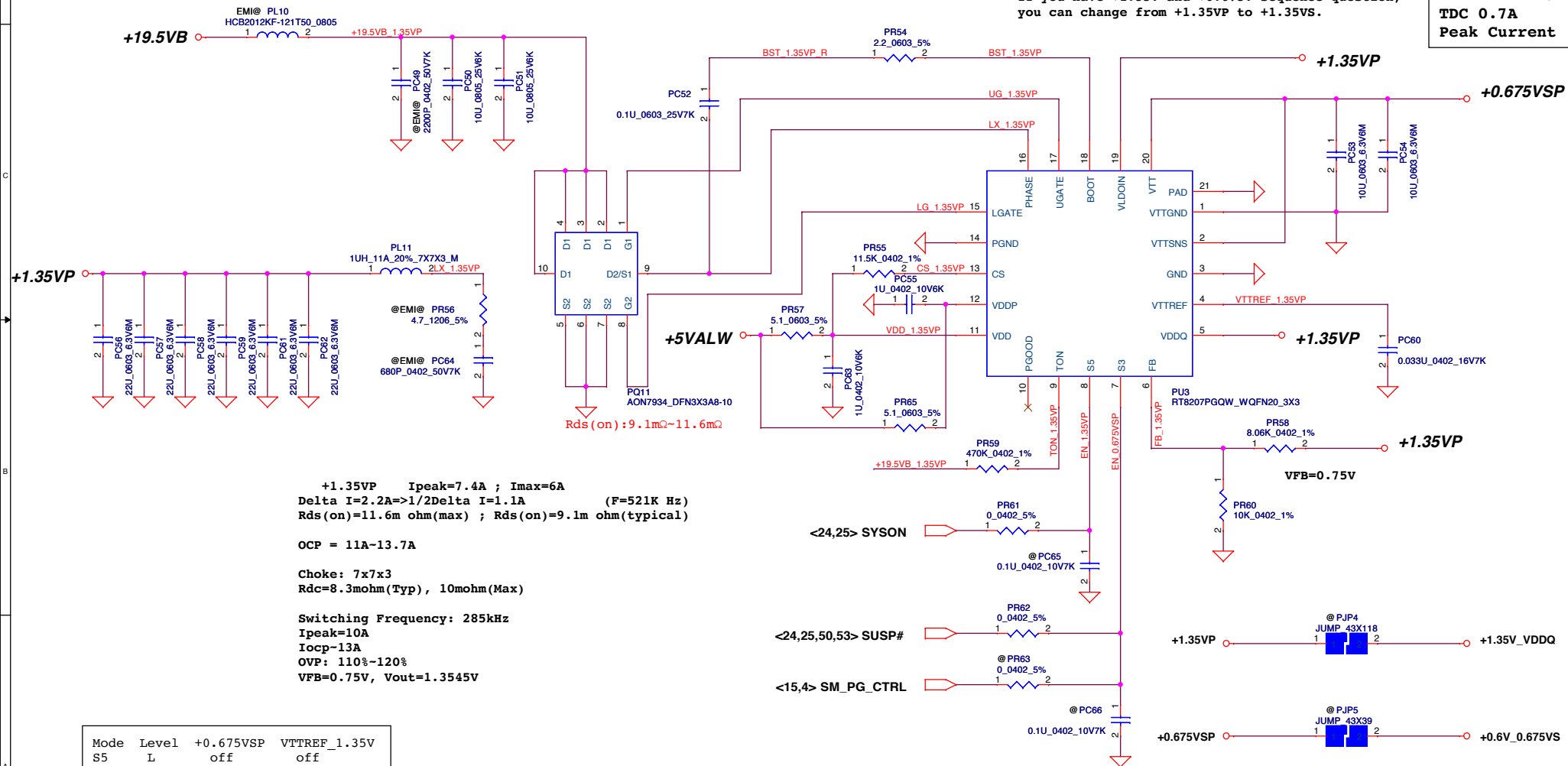
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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title 3VALW/5VALW			
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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



+1.35VP Ipeak=7.4A ; Imax=6A
Delta I=2.2A=>1/2Delta I=1.1A (F=521K Hz)
Rds(on)=11.6m ohm(max) ; Rds(on)=9.1m ohm(typical)

OCP = 11A-13.7A

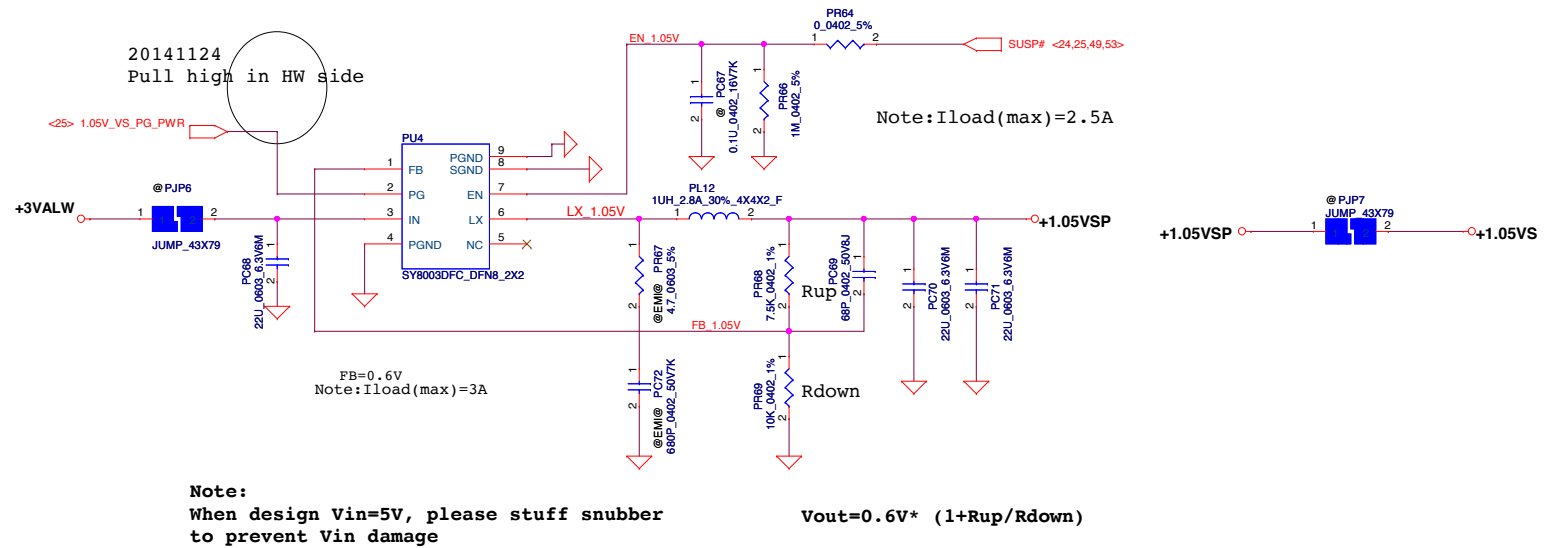
Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp=13A
OVP: 110%-120%
VFB=0.75V, Vout=1.3545V

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Issued Date	2010/07/20	Deciphered Date	2012/12/31	Title	RT8207P
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Module model information

SY8003_V2.mdd



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								SY8003	
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Size		Document Number						Rev	
Custom								0.1	
Date:		Saturday, January 31, 2015				Sheet		50 of 60	

Module model information:
ISL95813_V1A for IC module
ISL95813_V1B for SW module

Base on BDW PDDG Rev_0_73

Location	15W	28W	Note
	TDC 14A MAX 32A OCP 39A Loadline=-2.0mv/A	TDC 19A MAX 40A OCP 48A Loadline=-2.0mv/A	
PR89	287 Ohm	348 Ohm	OCP
PR85	1.27kOhm	1.58kOhm	Droop
PC88	0.033uF	0.01uF	RC Match
PR72	90.9kOhm	113kOhm	PROG1
PR75	95.3kOhm	95.3kOhm	IMON
PC83	0.1uF (0402)	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.15UH (Size:7*7*4)
Rdc=0.66mohm +-7%
Heat Rating Current=36A

+1.05VS

Follow intel guideline

Note:
VR_SVID_ALERT# Pull high on HW side

<1> VR_SVID_DAT

<1> VR_SVID_ALERT#

<1> VR_SVID_CLK

<1> VR_ON

<1> VGATE

Note:
VR_HOT# Pull high on HW side

<2> VR_HOT#

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92V, recovery

<1> VCCSENSE

<1> VSSSENSE

Local sense put on HW site

Note:
PR72=90.9K
=>Icc(max)=33A
fsw=700KHz

Note:
PR81=124K
=>Slew rate=53mV/us
Vboot = 1.7V

RC Match

OCP Setting

20150107
change PC88 PN
from SE0000060M8 to SE000006000

CPU_B+

+19.5VB

+VCC_CORE

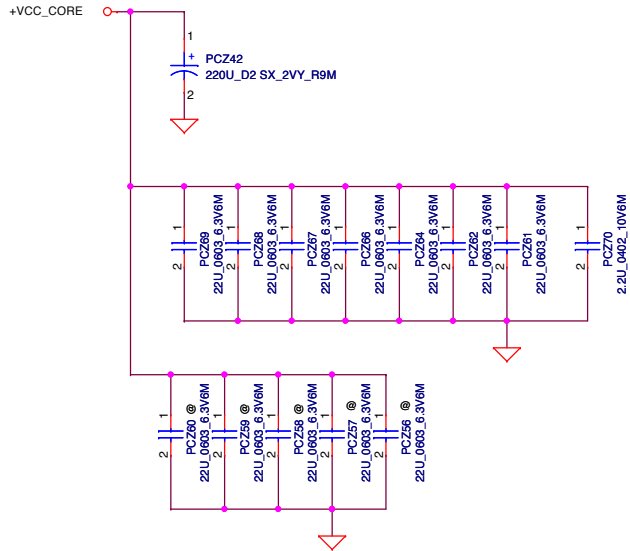


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ISL95813 for BDW-Y&U(15W/28W) CPU

LA-C701P

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BDW-U 15W
220uF x 1
22uF x 7
2.2uF x 1

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Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title	PROCESSOR DECOUPLING
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GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	VDDC
VID5	VID4	VID3	VID2	VID1	
0	1	1	1	0	1.150V
1	0	0	0	0	1.100V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V

Vboot(merge)

- Remark:
- PWM3 (Pin24) tie to 5V & CLK# (Pin40) external pull high
=> 2 phase GPU VR config
PWM3 (Pin24) tie to 5V & CLK# (Pin40) tie to GND or floating
=> 2 phase GPU VR config
 - When 2 Phase GPU config
a. DPSLPVR (Pin39)=0 PS# (Pin2)=0
=>1 phase CCM operation mode
b. DPSLPVR (Pin39)=0 PS# (Pin2)=1
=>2 phase CCM operation mode
c. DPSLPVR (Pin39)=1 PS# (Pin2)=0 or 1
=>1 phase DE operation mode

20150129
unpop PCB01 for lose dGPU issue

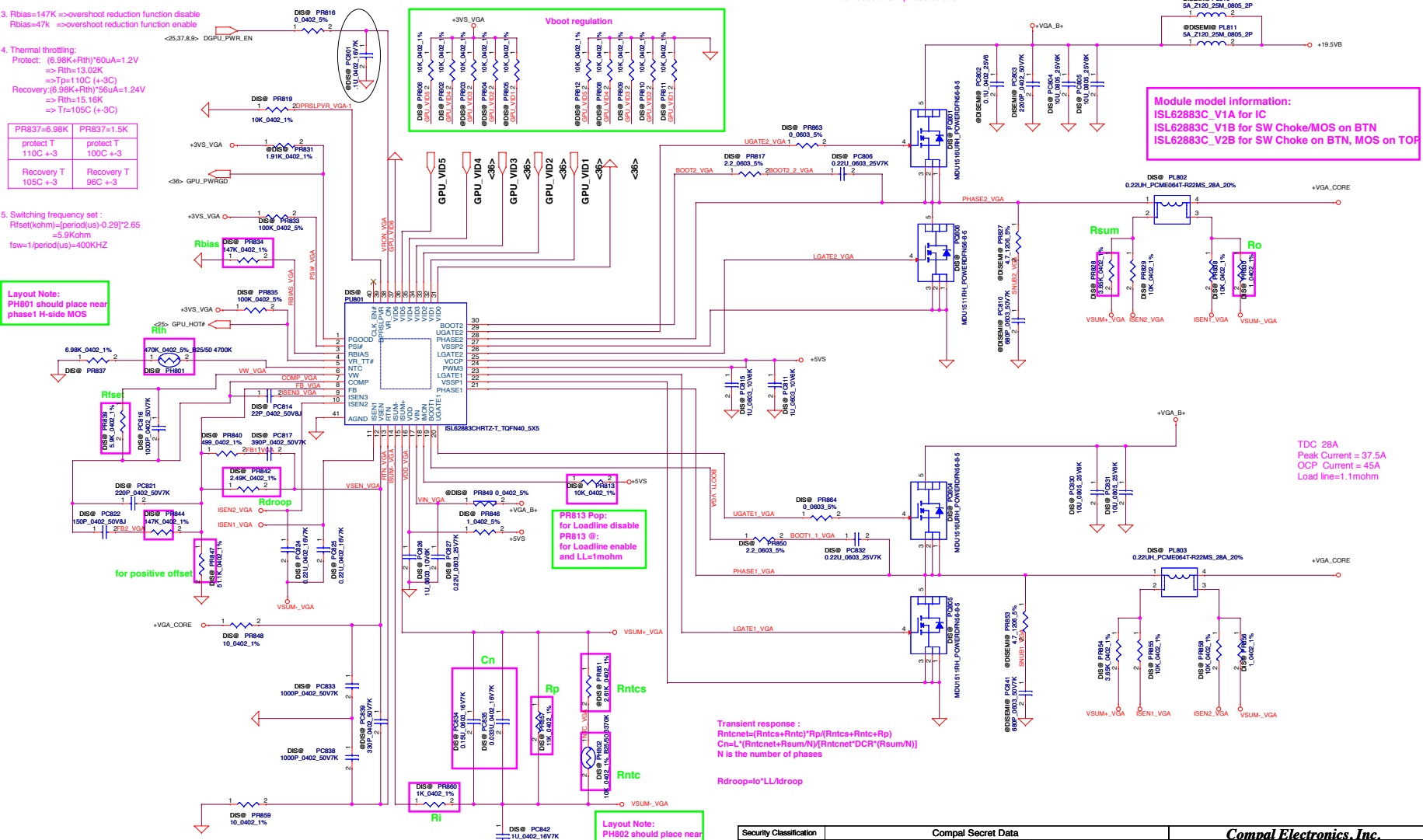
	AMD MARS series				AMD SUN series			Description
	LP: DDR3 PioXTXTX: GDDR5				UL: DDR3 PioXTXTX: GDDR5			
GPU	MARS XTX	MARS XT	MARS PRO	MARS LP	SUN UL	SUN PRO	SUN XT	NA
VDDC	0.775-1.175V	0.775-1.125V	0.775-1.050V	0.775-1.000V	0.775-1.125V	0.800-1.075V	0.800-1.150V	NA
TDC	32A (TDC)	25A (TDC)	21A (TDC)	17A (TDC)	16A (TDC)	19A (TDC)	25A (TDC)	NA
EDC	48A	37.5A	31.5A	26A	24A	28.5A	37.5A	NA
OCP	57.6A	45A	37.8A	31.2A	28.8A	34.2A	45A	NA
Vboot	0.85V	0.85V	0.85V	0.85V	0.9V	0.9V	0.9V	NA
Load line	1mohm	1mohm	1mohm	-----	-----	-----	1mohm	NA
Ri	1.13K Ohm	887 Ohm	750 Ohm	-----	-----	-----	887 Ohm	for OCP and LoadLine Setting
PR860	1.13K Ohm	887 Ohm	750 Ohm	-----	-----	-----	887 Ohm	for LoadLine Setting
Rdroop	1.43K Ohm	1.13K Ohm	953 Ohm	-----	-----	-----	1.13K Ohm	for LoadLine Setting
PR844	187K Ohm	147K Ohm	124K Ohm	-----	-----	-----	147K Ohm	for Compensation
PR847	51.1K Ohm	51.1K Ohm	51.1K Ohm	-----	-----	-----	51.1K Ohm	for Positive offset

H-side MOS:MDU1516
Rds(on):
9mohm@Vgs=10V
7.8-9mohm@Vgs=4.5V
Id:11A@Ta=25 degC

L-side MOS:UDU1511
Rds(on):
2.4mohm@Vgs=10V
2.7-3.3mohm@Vgs=4.5V
Id:24A@Ta=25 degC

Choke: 0.22uH (Size:7*7*4)
Rdc=0.98mohm +-5%
Heat Rating Current=28A
Saturation Current=28A

Remark: MARS LP/ SUN UL/ SUN PRO
don't use this 2-phase solution



Module model information:
ISL2883C_V1A for IC
ISL2883C_V1B for SW Choke/MOS on BTN
ISL2883C_V2B for SW Choke on BTN, MOS on TOP

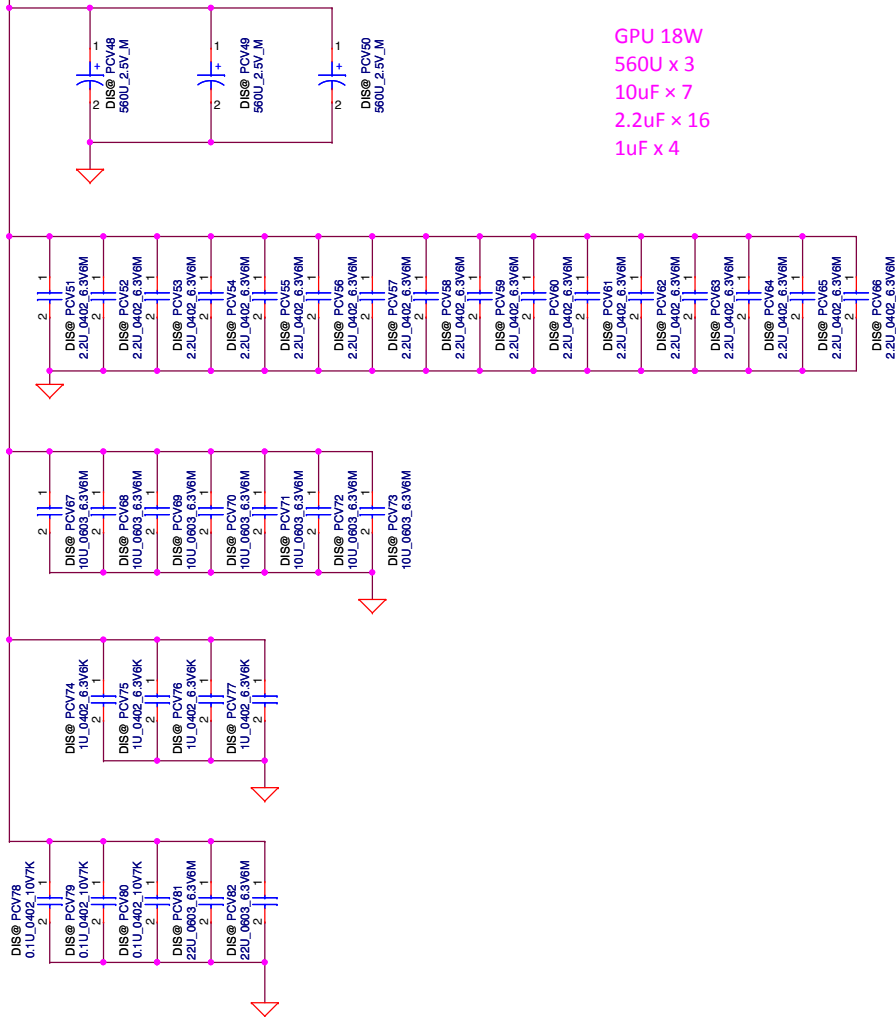
TDC 28A
Peak Current = 37.5A
OCP Current = 45A
Load line=1.1mohm

Transient response :
 $R_{ntcnet} = (R_{ntcs} + R_{ntc}) \cdot R_p / (R_{ntcs} + R_{ntc} + R_p)$
 $C_{nL} = [R_{ntcnet} + R_{sum} / N] / [R_{ntcnet} \cdot DCR \cdot (R_{sum} / N)]$
N is the number of phases

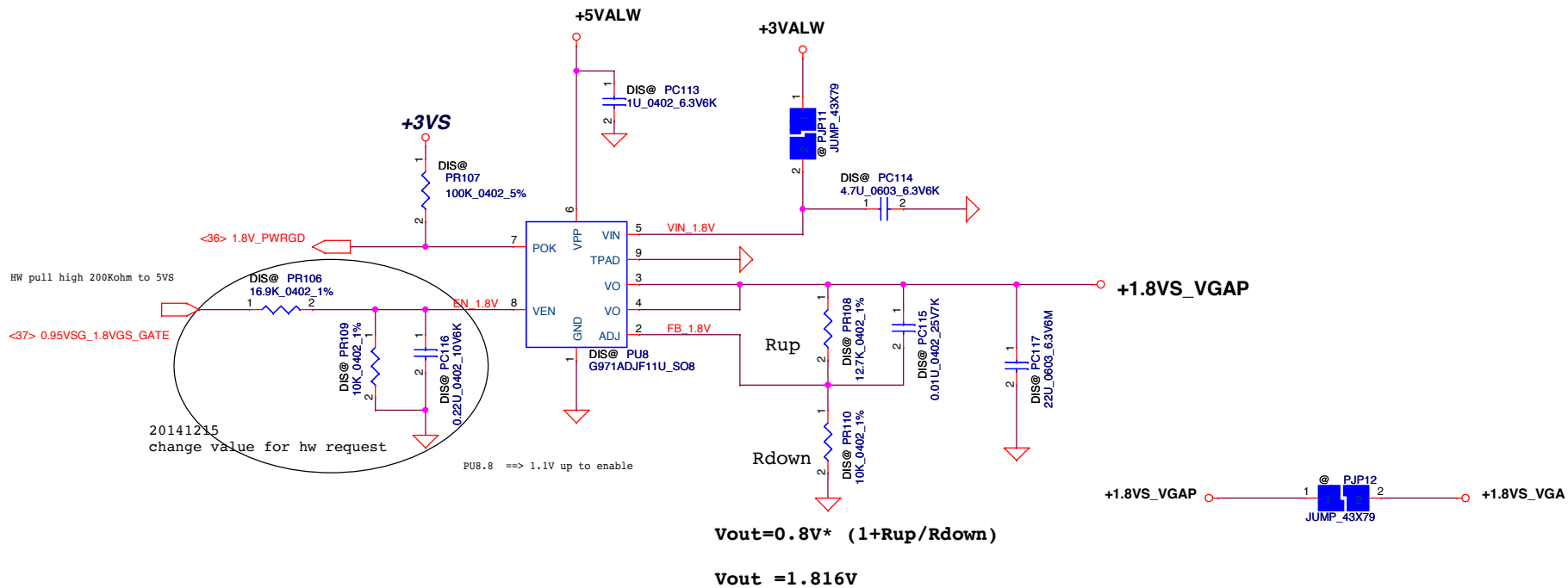
$R_{droop} = \rho \cdot L / droop$

Layout Note:
PH802 should place near
Phase1 Choke

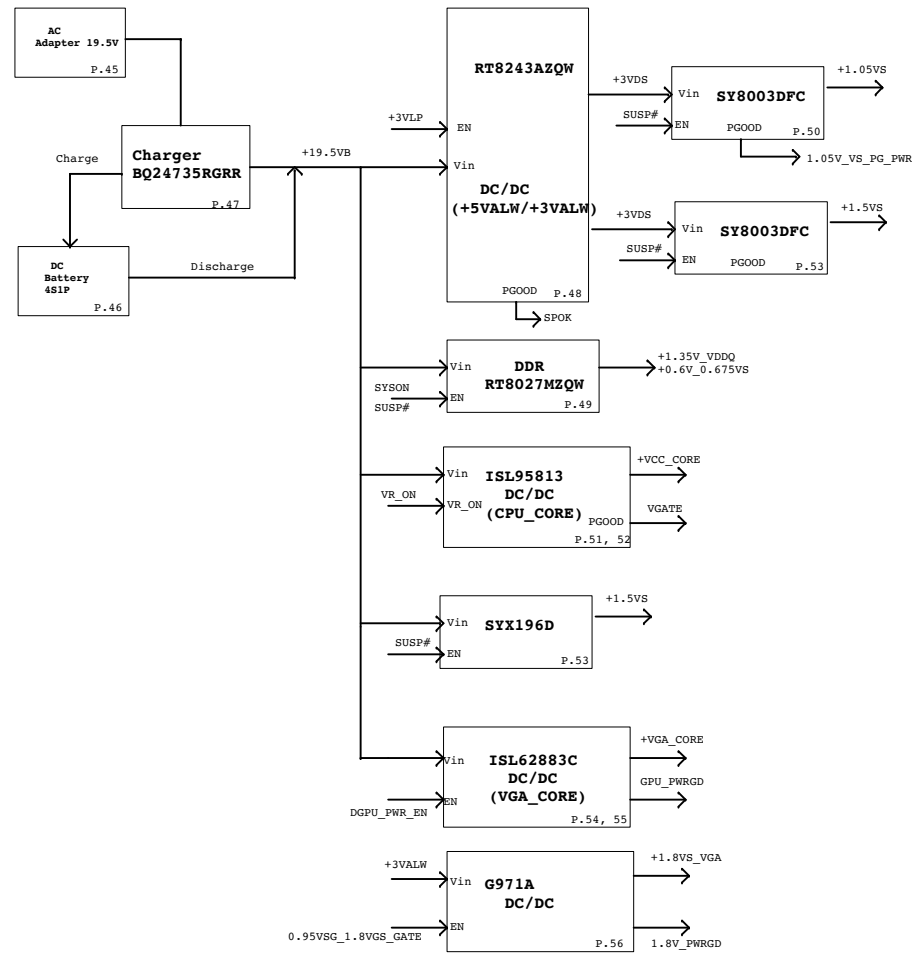
+VGA_CORE



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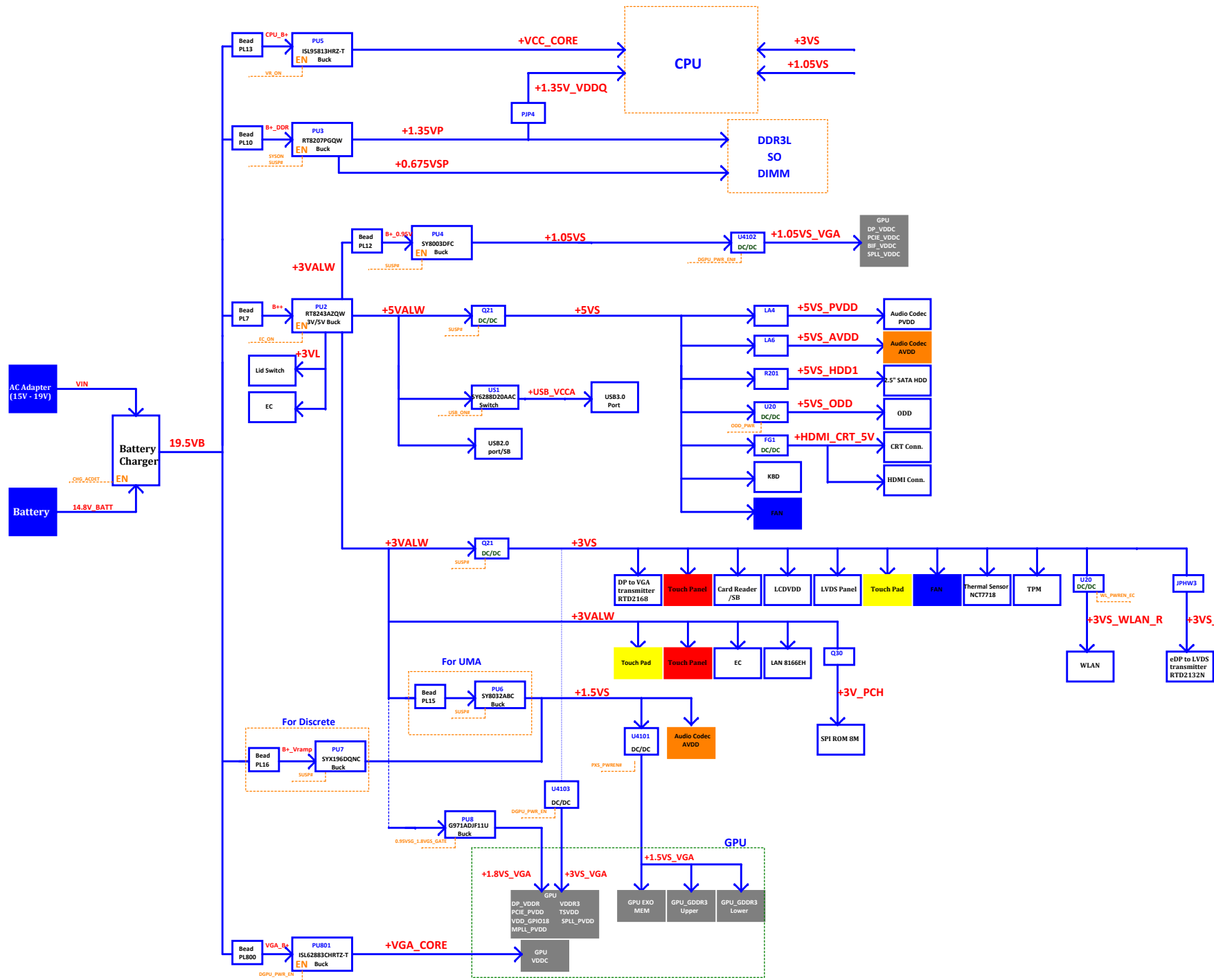


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LA-C701P			0.1
Revision History			Rev
001			0.1

Version change list (P.I.R. List)												
Item	Date	Fixed Issue	Reason for change	Modify List			Phase					
1	change size		use common part for 7x7	change PL202 size from 10x10 to 7x7			SI					
2	change part		no need 0ohm	PR224 and PR225 change from 0ohm to short pad			SI					
3	change part		HW request	Change R, C value PR106 100k => 16.9k PR109 47k => 10k PC116 0.1U => 0.22U			SI					
4	change part		Change PN	PC88 from SE0000060M8 to SE000006000			PV					
5	20150129		for lose dGPU issue	unmount PC801			PV					



Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
1	2014-11-25		A32 request	[A32] Reserve XDP circuit	DB
2	2014-11-25		A32 request	[A32] Reserve SMBUS from CPU to TP module	DB
3	2014-11-25	BDW CPU ESD issue	BDW CPU ESD issue solution	[Compal] Reserve Capx19 & Varistor x13 for BDW CPU ESD issue	DB
4	2014-11-25	[HP] Reserve XDP circuit	A32 request	[A32] eDP to VGA solution Sanrio--ITE IT6513 Candy--RTD2168	DB
5	2014-11-25		A32 request	[A32] KBC solution solution Sanrio--ENE KBC9012 Candy--ENE KBC9022	DB
6	2014-11-25		reduce component	[Compal] Remove WLAN LED circuit ,use KBC GPIO	DB
7	2014-11-25		A32 request	[A32] reserve TPM 1.2 & 2.0 TPM 1.2--SLB9665 TPM2.0--SLB9660	DB
8	2014-11-25		reduce component	[Compal] ODD load switch Sanrio use single load switch Candy use dual load switch	DB
9	2014-11-25		A32 request	[A32I] Change WLAN connector Sanrio--mini card Candy--M.2 Conn	DB
10	2014-11-25		reduce component	[Compal] Sanrio use power switch for Fan control , Candy use PWM control from KBC	DB
11	2014-11-25		A32 request	[A32] Card reader solution Sanrio--RTS5239 Candy--RTS5141	DB
12	2014-11-25		A32 request	[A32] GPU solution Sanrio--Nvidia N15V-GM (17W) Candy--AMD Exo pro (18W)	DB
13	2014-11-25		reduce component	[Compal] +3VS to +3VS_VGA from dual load switch to single load switch +1.8VS_VGA power direct support	DB
14	2014-12-14		For LAN 1V regout	[Compal] Pop LL3	SI
15	2014-12-14		For fine turn DGPU power sequence	[Compal] Change C4122 value from 0,01u to 0.22u	SI
16	2014-12-14		For fine turn DGPU power sequence	[Compal] Change R4109 value from 200K to 6.98K	SI
17	2014-12-14		For fine turn DGPU power sequence	[Compal] Change C4109 value from 0,01u to 0.027u	SI
18	2014-12-14		Modify WLAN PCIE CLK request channel	[Compal] Modify WLAN CLK request channel from 2 to 5.	SI

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Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
19	2014-12-14		Modify DGPU PCIE CLK request channel	[Compal] Modify DGPU CLK request channel from 3 to 4.	SI
20	2014-12-14		Modify LAN PCIE CLK request channel	[Compal] Modify LAN CLK request channel from 0 to 2.	SI
21	2014-12-23		HP request add thermal sensor for CPU PCB.	[Compal]Add CPU external Thermal sensor at EC_SMB_CK2/DA2.	SI
22	2014-12-23		CPU and GPU thermal sensor can't on the same bus.	GPU thermal sensor change to EC_SMB_CK3/DA3	SI
23	2014-12-23		Modify EC co-lay pin117 & 124.		SI
24	2014-12-24		EMI request to change HDMI schematic.		SI
25	2014-12-25		Reserved +5VS Touch power.		SI
26	2015-01-26		BIOS request.	Add pull-up at PCIECLKREQ1#	PV
27	2015-01-27		SVTP 3-9 fail.	R38 power change to +HDMI_CRT_5V , L7,L8,L9 change P/N.	PV
28	2015-01-27		SVTP 3-9 fail.	Remove Hsync,Vsync Buffer footprint.	PV
29	2015-01-28		Reserved for test.	Reserved 0 ohm on ODD_PLUG# , between CPU and ODD.	PV
210	2015-01-30		EMI request	Add 680p at PWR_LED#	

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